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MT6516 Design Notice V1.0

2009 / April

WCP/SA

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Change Notice

- 2009/05/11 Initial document
- 2009/06/22 Add IQ 510ohm

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Outline

- MT6516 Main Features & Package
- Design Notice
  - MT6516 schematic design notice
  - PMIC MT6326 design notice
  - Audio part design notice
  - Speech part design notice
  - Camera design notice
  - Display design notice
  - DDR memory layout rule
  - USB 2.0 high speed design notice
- Factory Mode and Engineer Mode
- Download and META Link
- MT6516 Memory Support Plan
- Appendix - Peripherals Design Notice
  - WIFI/BT Co-module Application Note
  - MT3326 GPS application note
  - DTV part design note
  - FM design notice

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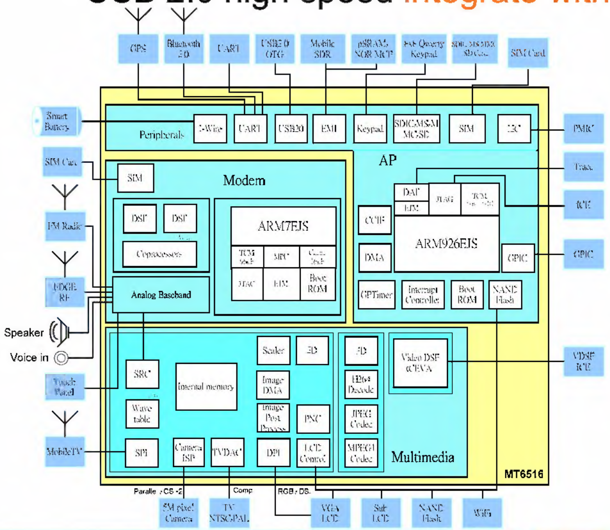
MT6516 Main Feature

- Separate Application (ARM9) and hard real-time Modem (ARM7)
- Multi-Cores with HW coprocessors SoC
  - Application: ARM926EJS 416MHz
  - Modem: ARM7 (52MHz/104MHz) + 2 DSP(104MHz)
  - CEVA DSP (312MHz) for video and unpredictable multimedia application on Smartphone
- 65nm process. Ultra low power design.
- Graphics, Display, Image, Camera, Video multimedia hardware accelerators.
  - 2D Graphics - support Window Mobile Bitblt function
  - 3D Graphics - Support OpenGL ES 1.1 Common/Common Lite profile
  - 3D Performance: fill rate = 32M, triangle rate = 3.7M
- Wide range of resolution up to WVGA size
- Various display Interface Support
  - 8080 host IF (MIPI DBI)
  - 8/9/16/32-bit Serial IF
  - RGB interface (MIPI DPI)
  - MIPI DSI interface
- High Performance Memory controller @ 104MHz, support
  - 32-bit / 16-bit LP-DDR SDRAM
  - 4 chip selects : support up to 4 DRAM devices
  - NAND-boot supported
  - NAND data storage supported
- Peripherals
  - Dual SIM
  - 3 x SDIO, 3 x I2C, 1 x I2S, 4 x UART
  - 1-wire interface, 7 x PWM
  - 8 x 8 Key Matrix
  - Touch panel interface
  - USB 2.0 high speed integrate with PHY.



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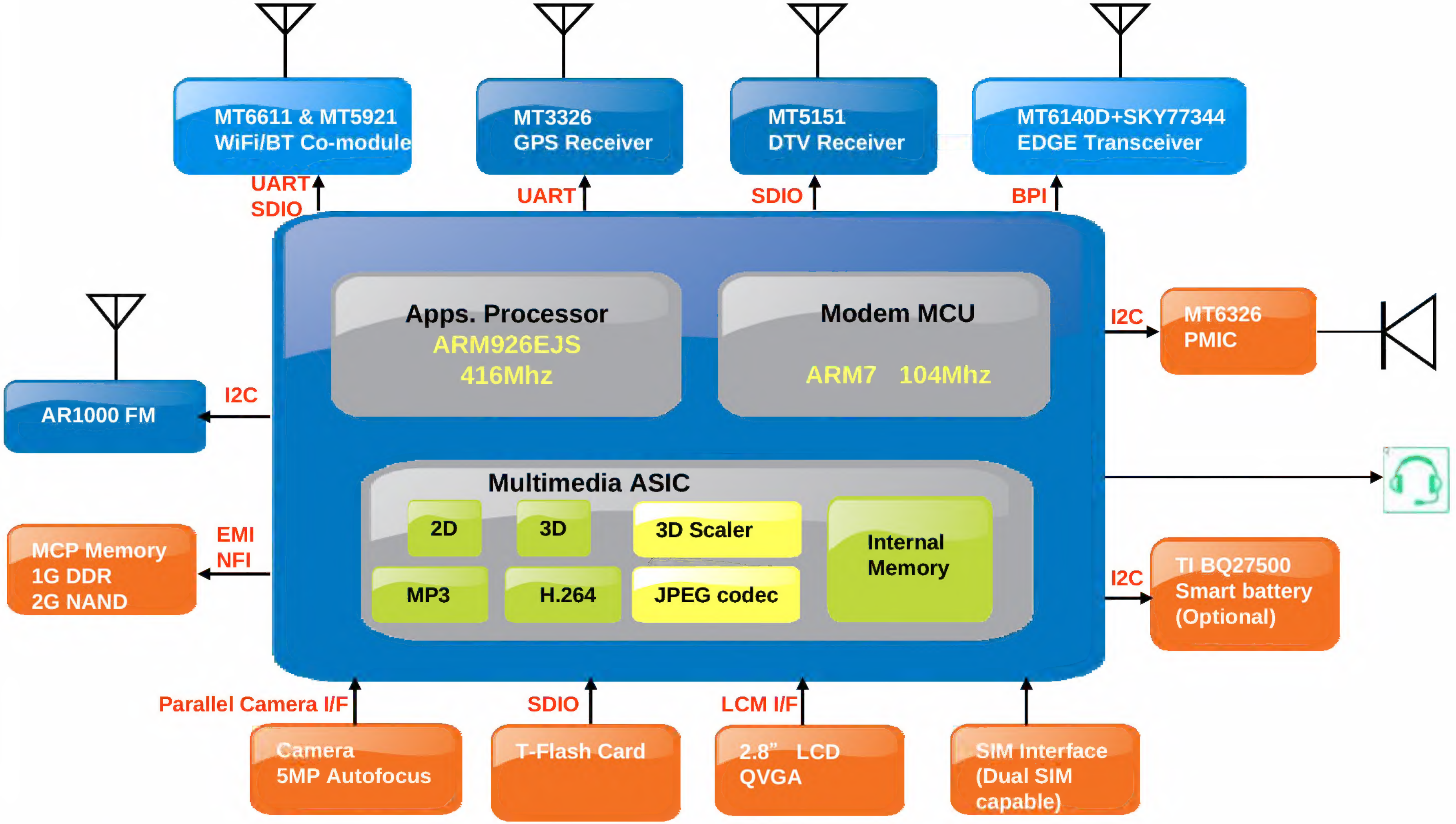
MT6516 Design Package Building Blocks



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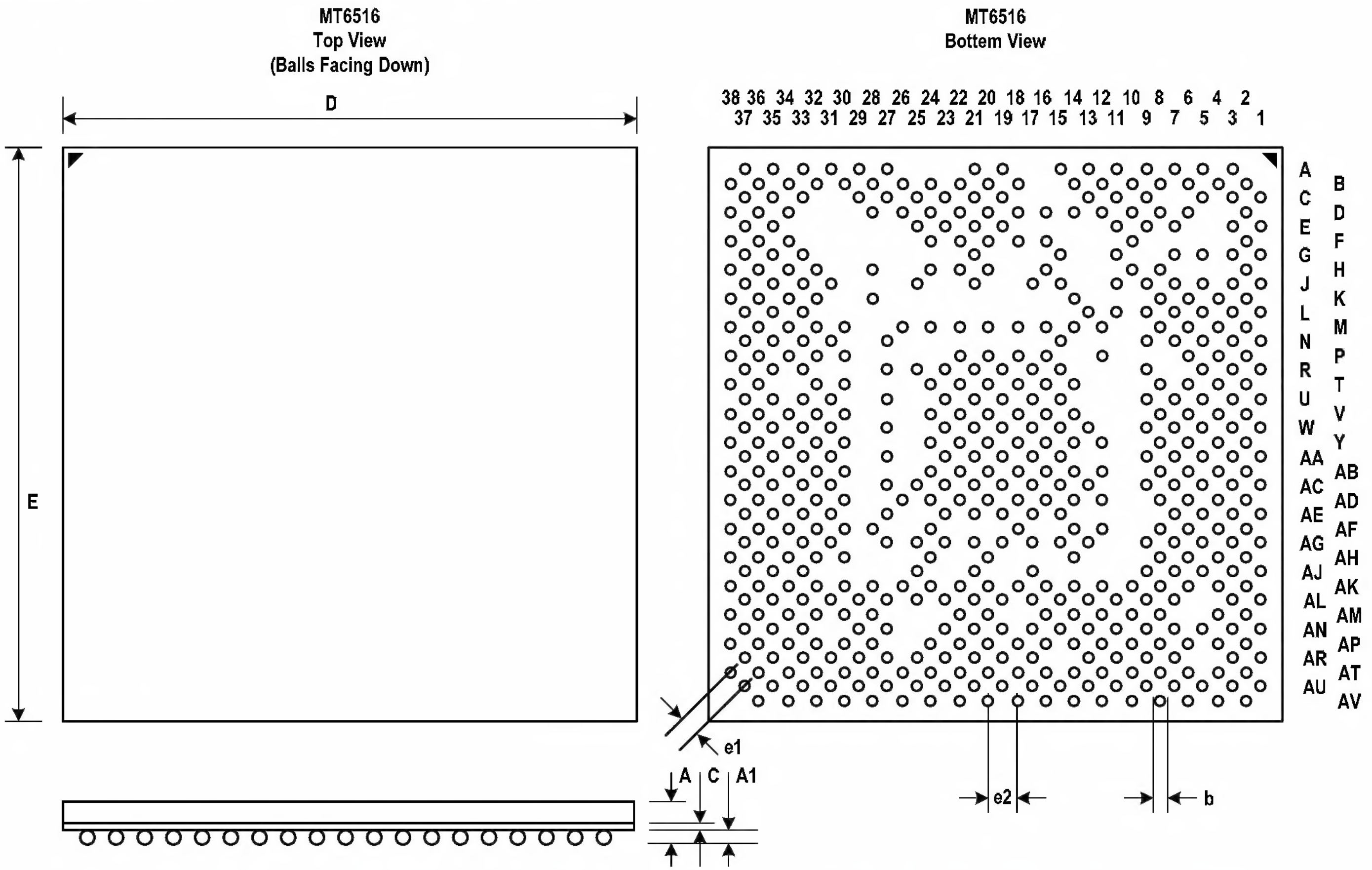
MT6516 Package



Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Substrate Thk.
D	E	N	e1 / e2	b	A (Max.)	A1	C
15	15	564	0.378 / 0.535	0.3	1.2	0.21	0.26

Table 1 Definition of TFBGA 15mm*15mm, 564-ball, 0.378 mm pitch Package (Unit: mm)

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Design Notice -
MT6516 Schematic Design Notice

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Schematic Notice (1/7): Boot-up selection

Pin H\L	H(DVDD)	L(GND)
IONEJTAG	Enable one JTAG functior	Disable
IBOOT	boot from external memor	boot from bootrom
SECU_EN	Enable secure booting	Disable
IADMUX	ADMux memory device	AD-Demux memory device
ICORESIGHT	Coresight enable,	Coresight disable
FSOURCE	burn efuse	Normal

- MT6516 currently only support DDR memory, so this selection always choose GND
- Connect FSOURCE to GND by **0ohm,** otherwise the UUID number will be **unstable.**

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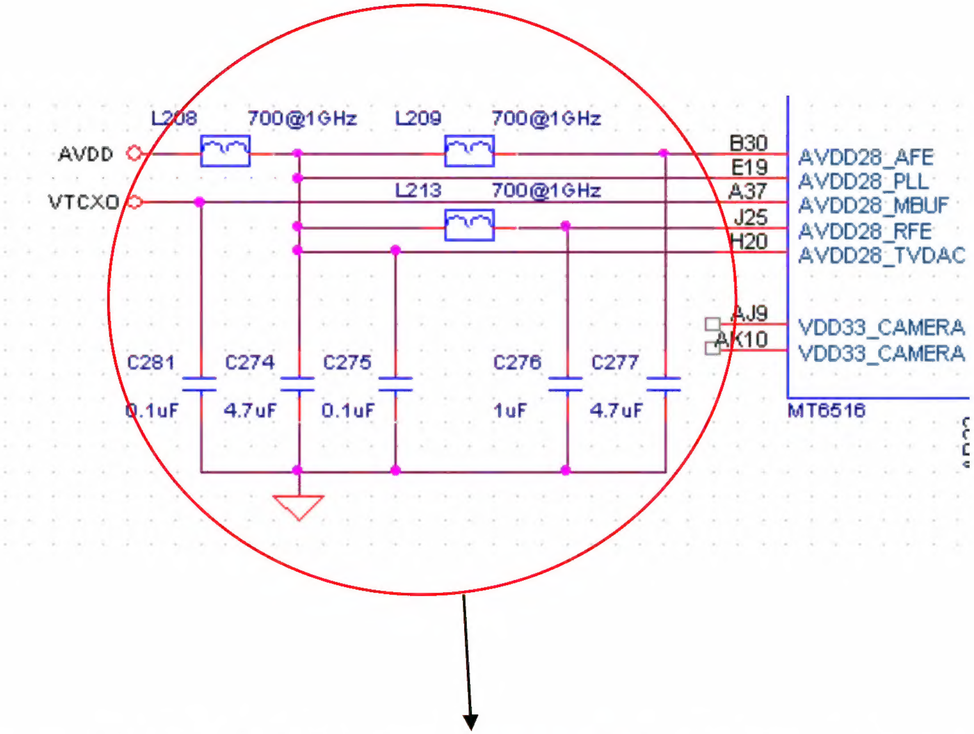
Schematic Notice (2/7)



The AVDD Power must follow the connection show above to avoid the influence between AFE, RFE and MBUF

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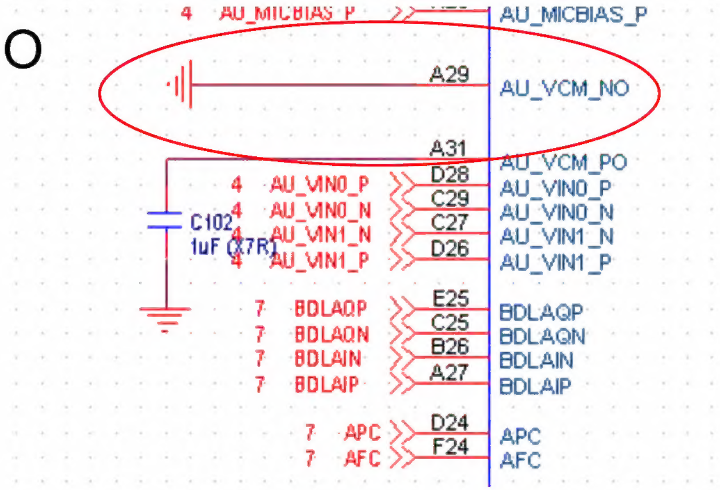
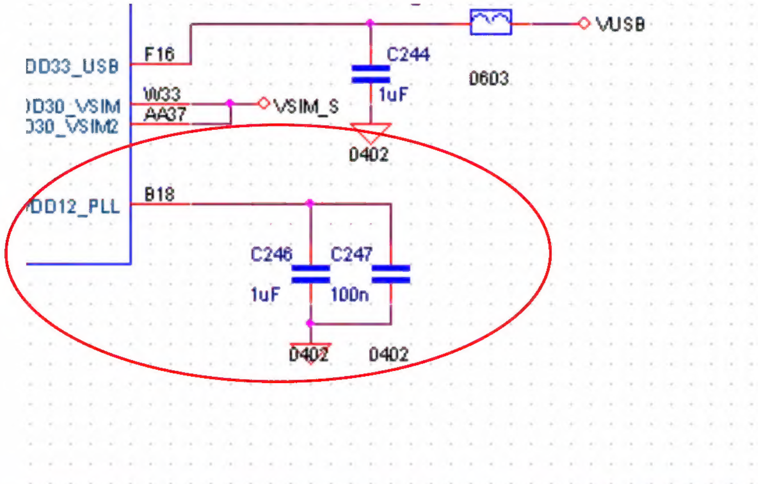
Schematic Notice (3/7)

Connect AU_VCM_NO to GND



Add 2 capacitors (1uF, 0.1uF) in AVDD12_PLL



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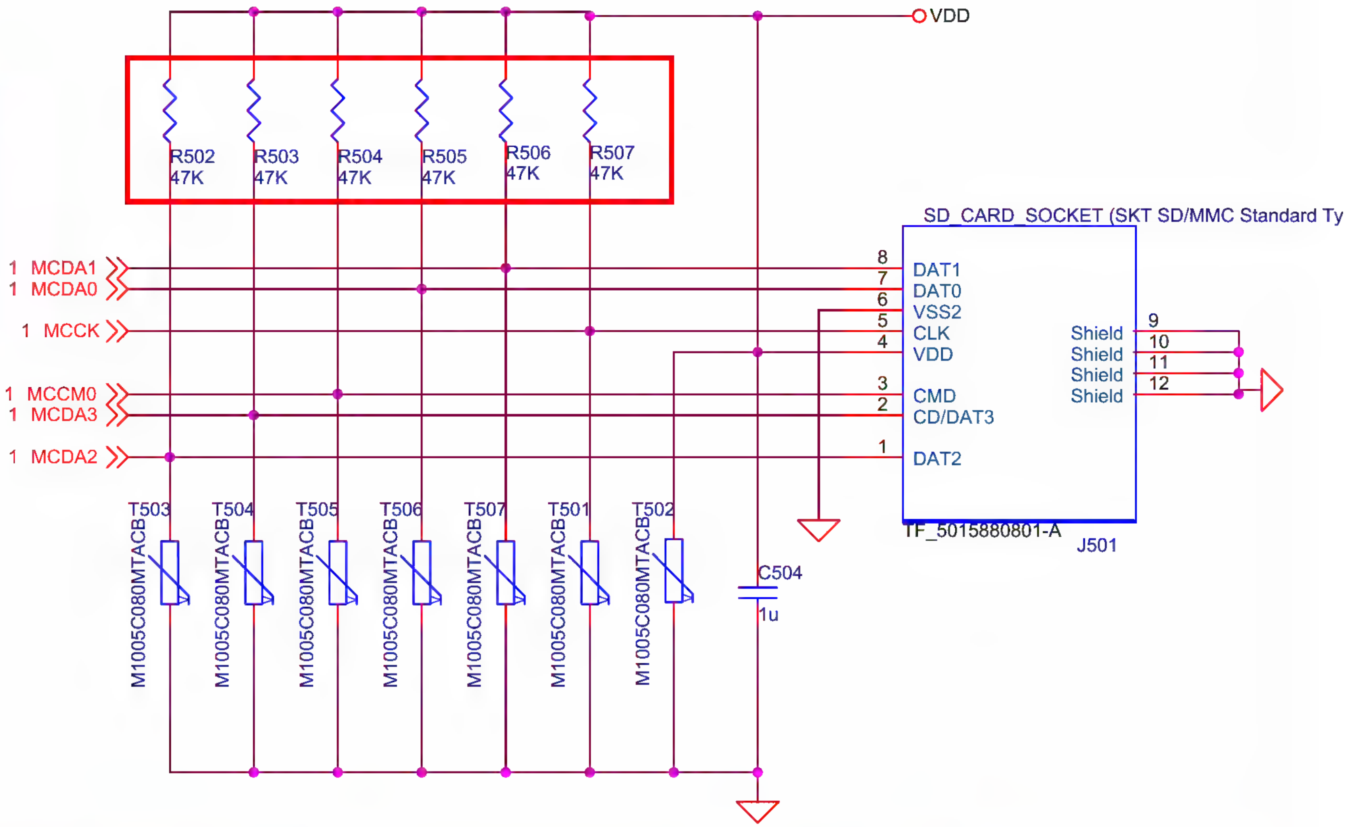
Schematic Notice (4/7)

•For better interoperability and stability, please reserve 47k ohm in each memory card interface line.



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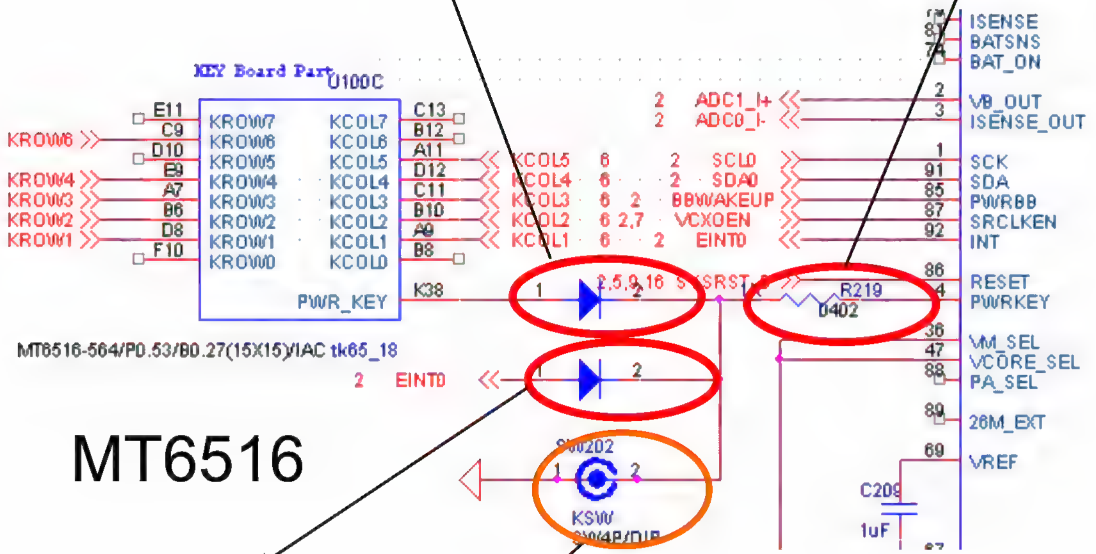
Schematic Notice (5/7)

Add a diode between MT6516 PWR_KEY and MT6326 PWRKEY

Add a 1k resistor to avoid ESD damage.



MT6516

Add a diode and a EINT to MT6326 PWRKEY

MT6326 PMIC

Power Key Bottom

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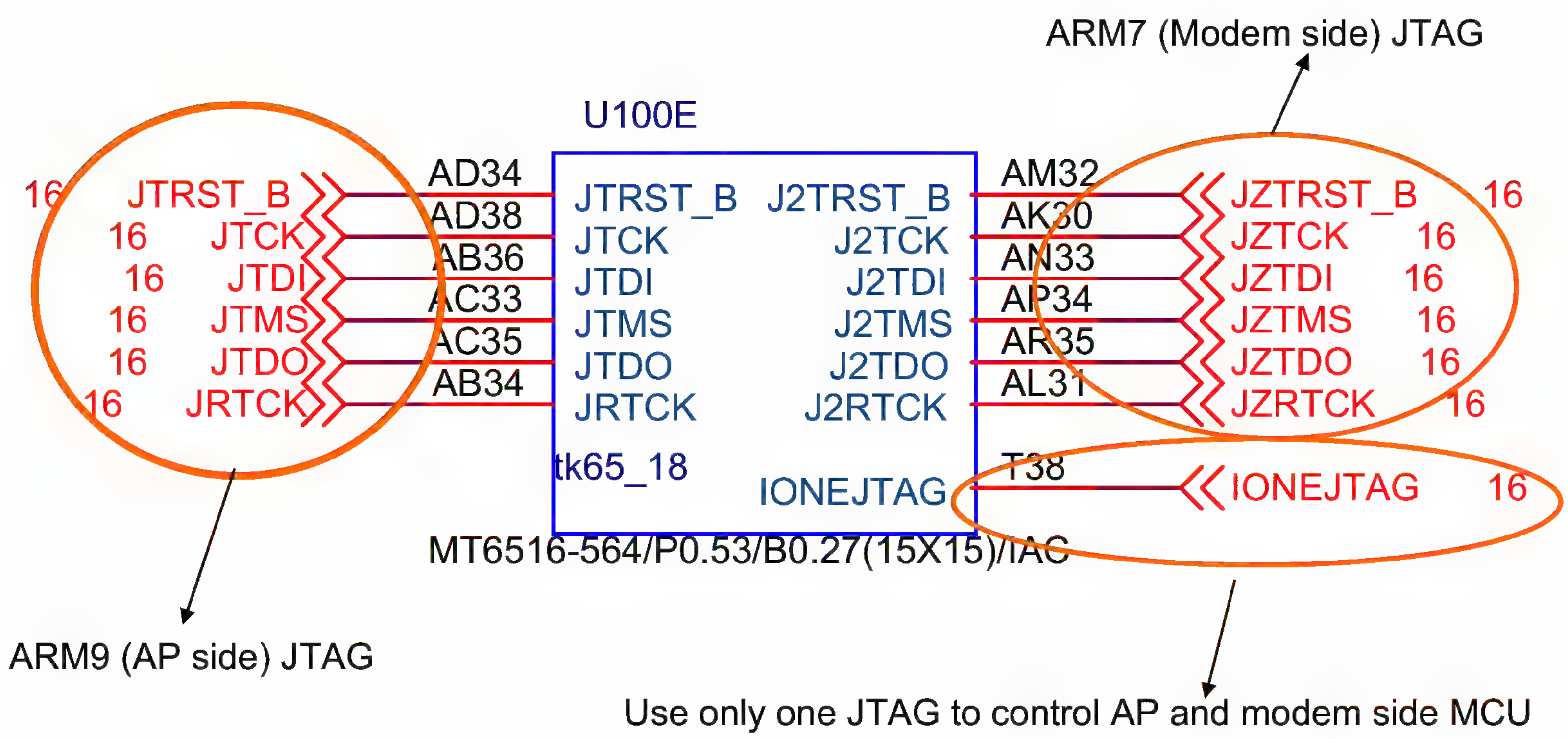
Schematic Notice (6/7) :Debug Port



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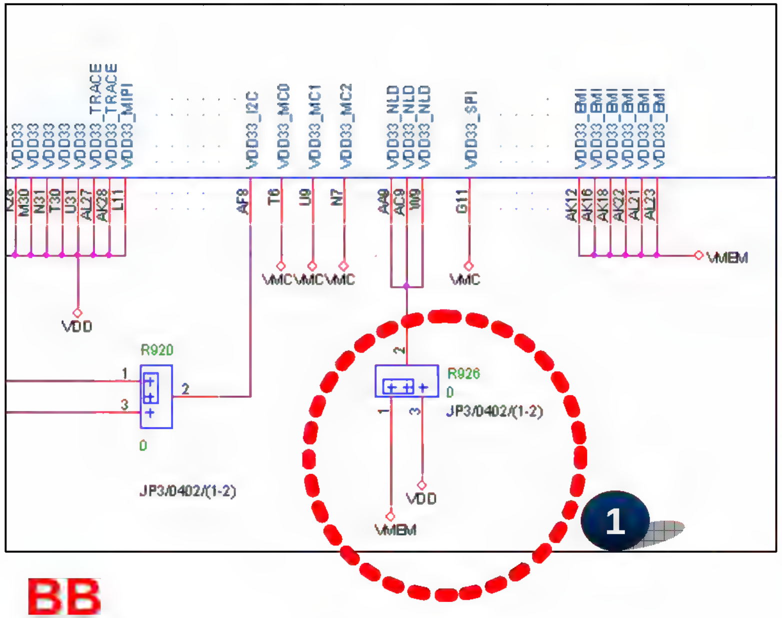
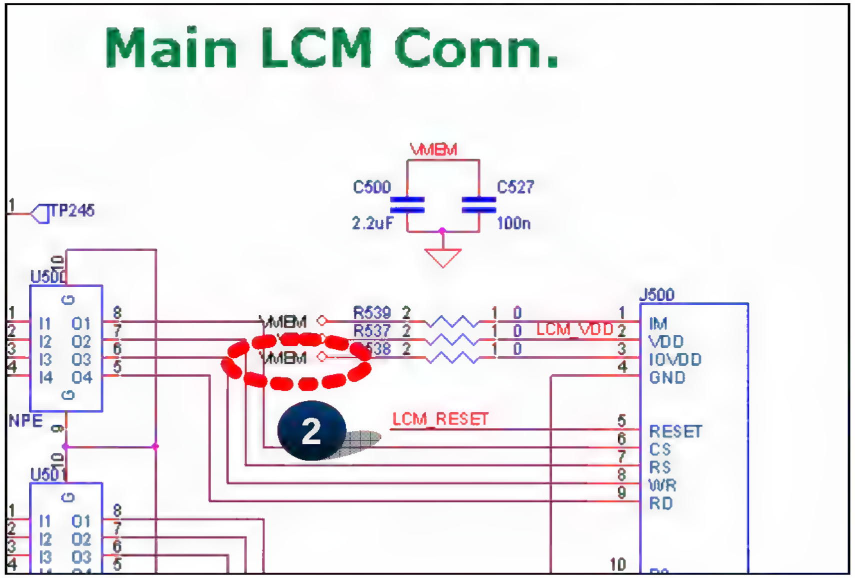
Schematic Notice (7/7) : NFI Interface

- To support 1.8 V NAND MCP, you need to
  - Connect VDD33_LCD of BB part to 1.8 V
  - Check if LCM module IO can support 1.8V first. Connect LCM IO power pin (VDDIO) to 1.8 V *(see <u>LCM Selection Guide to 1.8 V LCM</u> section)*



BB



LCM IO

• Beware that **NAND flash**, **parallel LCM**, and **VDD33_NLD** must use same power domain !

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RF IQ Connection (Remember add 510ohm Between Baseband and MT6140D)

Must add series 510R when using MT6516 or MT6268
This is also applied when PA is changed to RF3159

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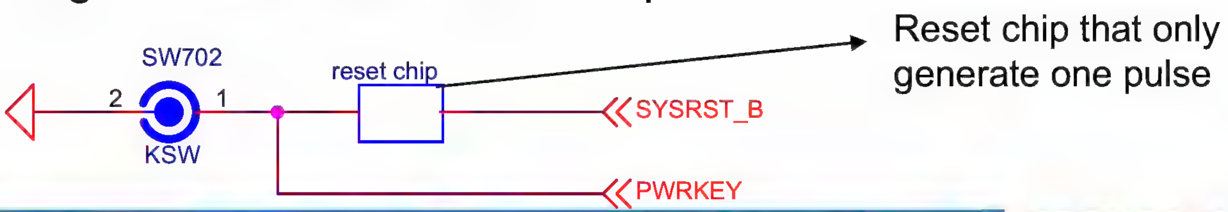
Reset Button Design Suggestion

1. Basically, the MT6516 phone don't need reset button. (Users remove battery when system hang)
2. There are two kinds of suggestion design of reset button.
   1. Only add a pull low button on SYSRST_B pin
      1. Advantage : cost effective
      2. Disadvantage : User must press **pwrkey** to restart system

   2. Add a reset chip on pwrkey pin and SYSRST_B pin.
      1. Advantage : User can press reset then direct restart the phone.
      2. Disadvantage : Need a extra reset chip



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Default UART Dispatch Notice

UART1	Download Bootloader, META Link, Production Line Test Point
UART2	User Define, Default Use for AGPS
UART3	User Define, Default Use for Bluetooth
UART4	Data Log for Debugging, Boot-Up Selection and Setting. Modem side META link.
USB Port	Download Image BIN file, Active Sync, Mass Storage, RNDIS

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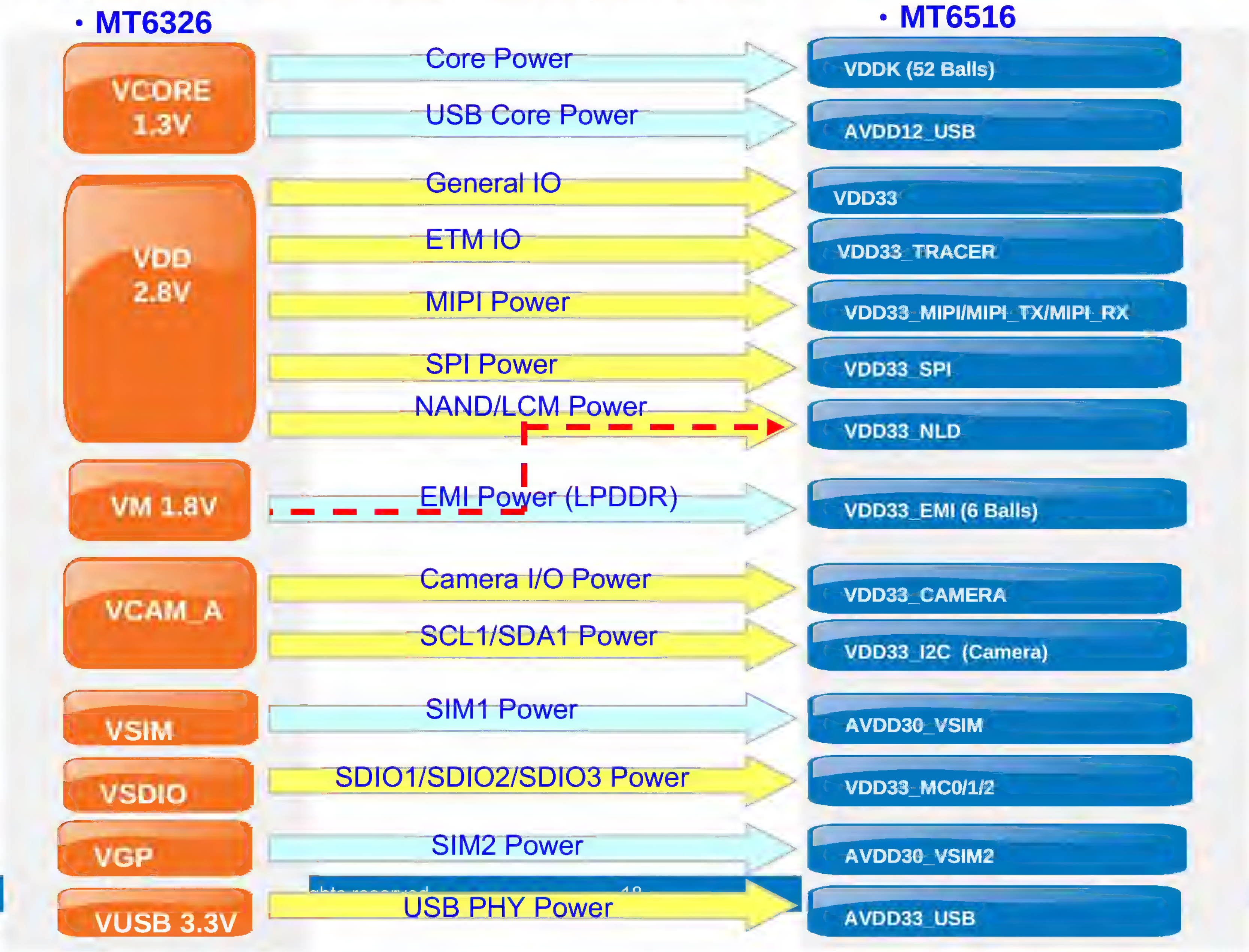
Reference Power Distribution



MT6516 reference phone PCB layer define

Layer No.	Name	Define	Material		Suggestion	Die. Con.	suggest thickness(mil)	Via
			SolderMask	SolderMask			0.4	
			Add Plating	plating				
1	COMP(L1)	RF Trace	Copper foil	0.5 oz	H oz+plating		1.4	
				PP	PP 1080 65%	4.3	2.82	
2	L2	Signal	Copper foil	1.0 oz	0.50 oz+plating		1.3	
				CORE	PP 1080 65%	4.3	2.82	
3	L3	GND	Copper foil	1.0 oz	Copper 1.0 oz		1.3	
				PP	FR-4 Core 4mil	4.3	4	
4	L4	RF Trace	Copper foil	1.0 oz	Copper 1.0 oz		1.3	
				CORE	PP 7628 50%	4.3	8.38	
5	L5	GND	Copper foil	1.0 oz	Copper 1.0 oz		1.3	
				PP	FR-4 Core 4mil	4.3	4	
6	L6	Signal	Copper foil	1.0 oz	Copper 1.0 oz		1.3	
				CORE	PP 1080 65%	4.3	2.82	
7	L7	Signal	Copper foil	1.0 oz	0.50 oz+plating		1.3	
				PP	PP 1080 65%	4.3	2.82	
8	SOLD(L8)	RF Trace	Copper foil	0.5 oz				
			Add Plating	plating	H oz+plating		1.4	
			SolderMask	SolderMask			0.4	
Board Thickness =1.00mm +/- 10%mm							39.06	

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MT6326 PMIC Design Notice

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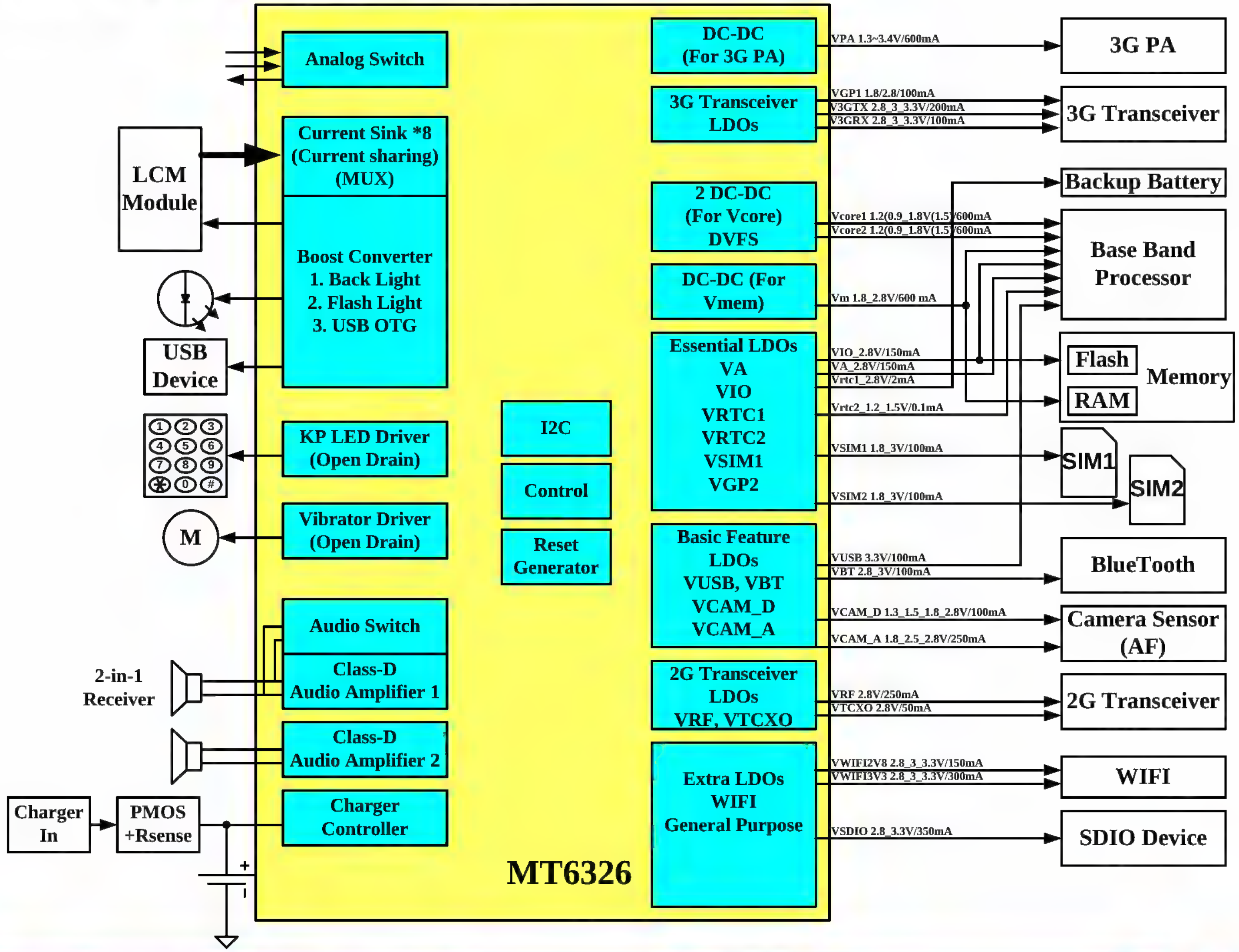
MT6326 PMIC



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MT6326 PMIC LDO

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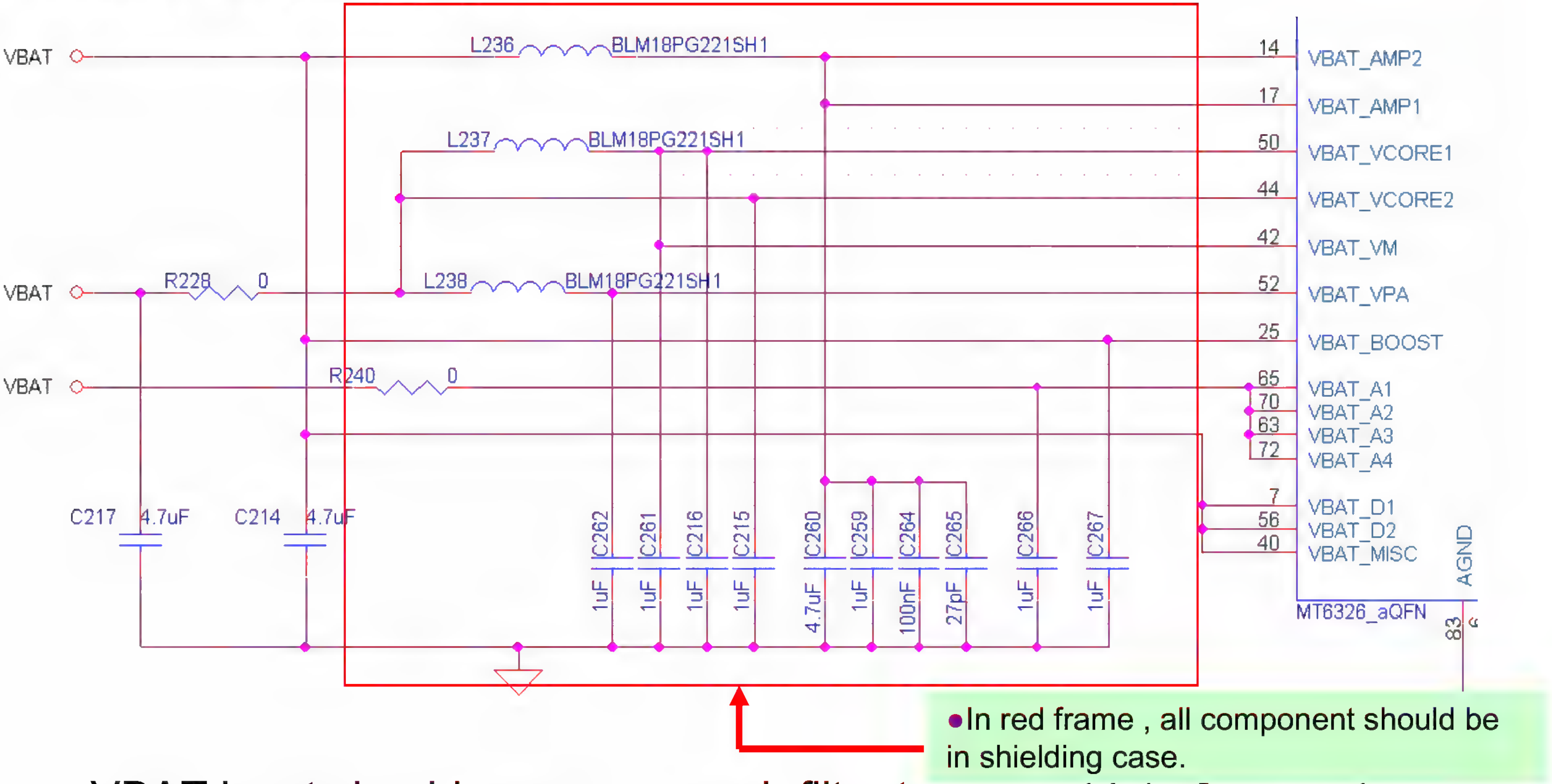
Regulator	Output Voltage	Output Current	Output Components	Notes
VCORE	**0.9~1.35** **1.8**	600	2.2uH + 4.7uF	Max. output current = 100mA when set to < 1.1V
VCORE 2	**0.9~1.35** **1.8**	600	2.2uH + 4.7uF	Max. output current = 100mA when set to < 1.1V
VM	**1.8** **2.8**	600	2.2uH + 4.7uF	Max. output current = 450mA when set to 2.8V
V3GPA	1.3~3.4	600	2.2uH + 4.7uF	VBAT should keep 600mV higher than V3GPA to keep good regulation.
V3GTX	2.5/2.8/3/3.3	200	4.7uF	
V3GRX	2.5/2.8/3/3.3	100	4.7uF	
VRF	2.8	250	4.7uF	
VTCXO	2.8	50	1uF	
VA	**2.8**	150	4.7uF	For AVDD, FM power requirement
VCAMA	1.5/1.8/2.5/2.8	250	4.7uF	
VWIFI3V3	2.5/2.8/3/3.3	300	4.7uF	
VWIFI2V8	2.5/2.8/3/3.3	150	4.7uF	
VIO	**2.8**	150	1uF	For VDD and peripheral I/O requirement
VSIM	1.8/3.0	100	1uF	
VUSB	**3.3**	100	1uF	
VBT	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	1uF	
VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	1uF	
VSDIO	2.8/3	300	4.7uF	
VGP1	1.3/1.5/1.8/2.5/2.8/3.0	100	1uF	
VGP2	1.3/1.5/**1.8**/2.5 2.8/3.0	100	1uF	
VRTC	1.5/1.2	0.1	1uF	
BAT_BACKUP	2.8	2	1uF	Backup battery

VBAT Input Filter



- VBAT input should reserve enough filter to prevent interference to RF performance.
- All above component should be as close to MT6326 IC as possible

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Class-D Audio Amplifier Output Filter

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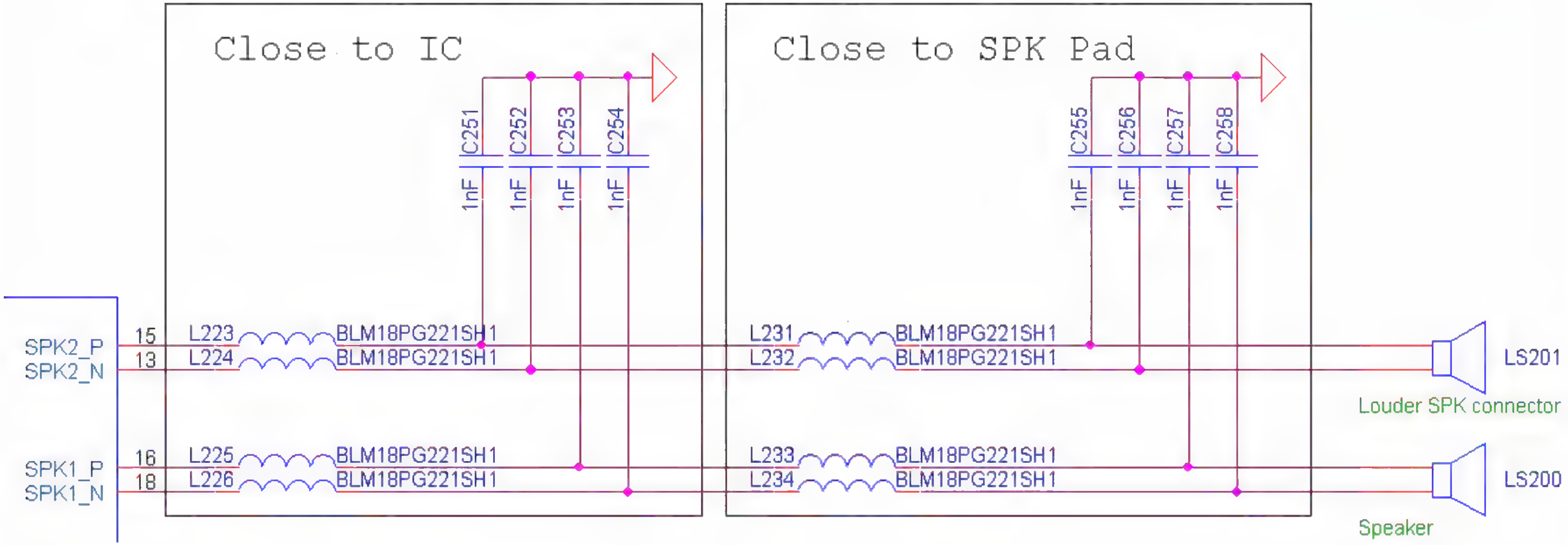

- Reserve 2 stage filter at output stage of Class-D to prevent interference to RF performance.
- 1st stage filter should be close to IC, 2nd stage filter should be close to loud speaker.
- All the traces from IC to 2nd stage filter should not exposed to prevent interference to RF performance.

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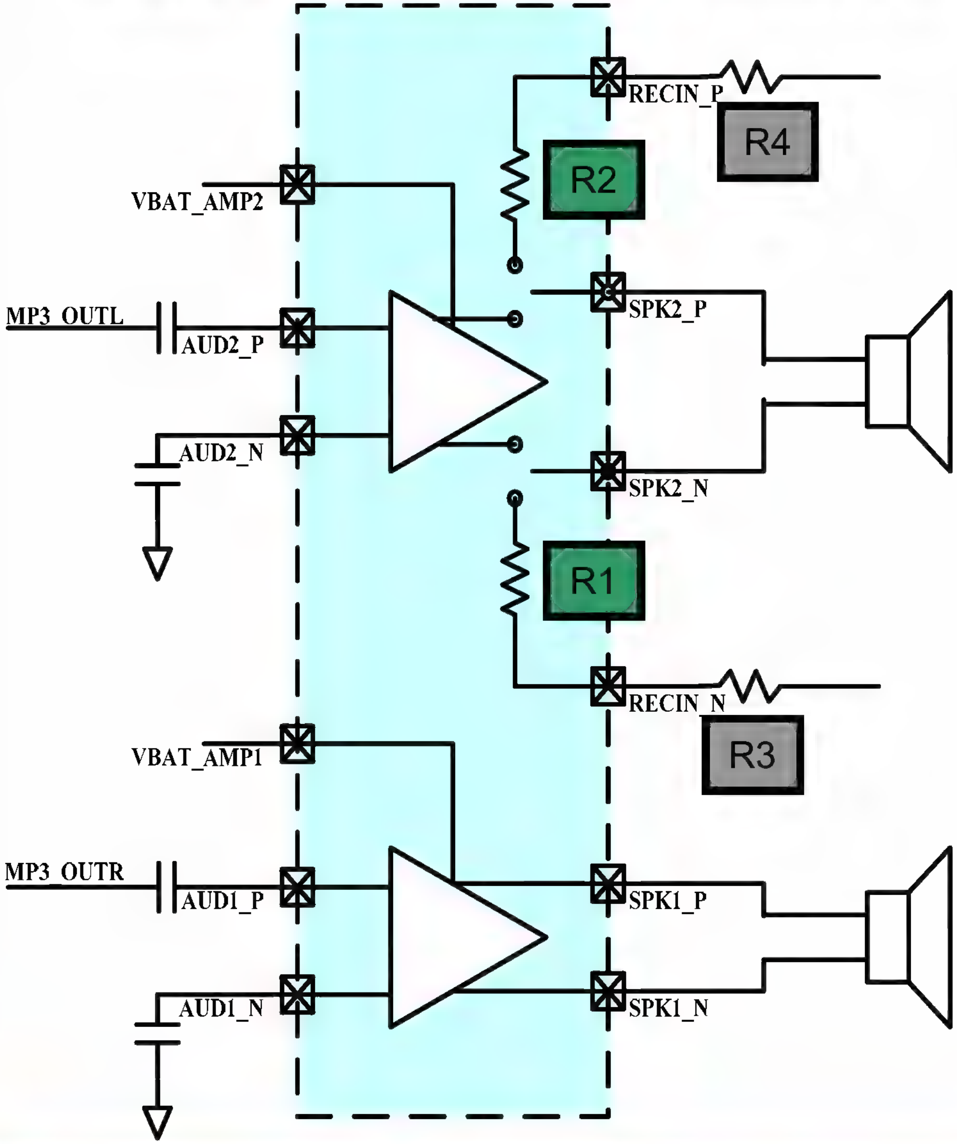
Class-D : 2-in-1 Receiver Function



- MT6326 has 2 in 1 receiver function , when use external amplifier , must connect RECIN_P and RECIN_N.
- The typical value of R1 and R2 are 20 ohm each , and suggest R3 and R4 to be 4 ohm (32–20–8=4)
- Due to value variation of R1 and R2 are higher , so maybe suffer audio volume.

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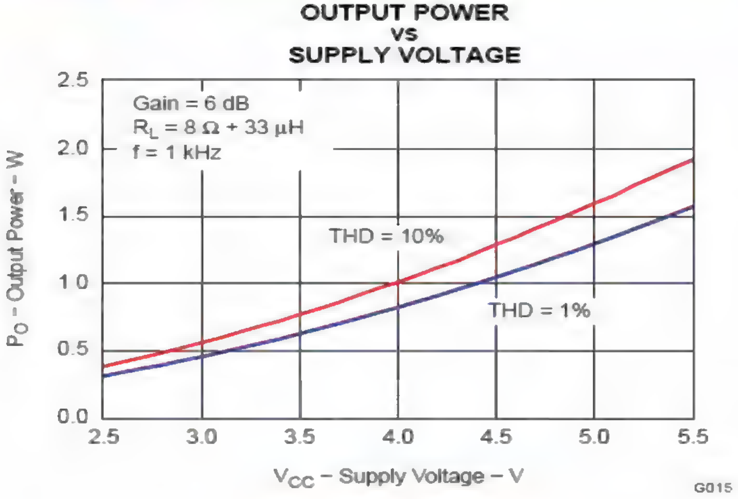
Class-D : Audio Amplifier Power Output

	MT6326 Class-D Ampilifer		TI TPA2016D2 Class-D Ampilifer	
Pomax Maximum output power	THD+N = 10%, VDD = 4.2 V, RL = 8 Ω	1.2 W	THD+N = 10%, VDD = 5 V, RL = 8 Ω	1.72 W
	THD+N = 10%, VDD = 3.3 V, RL = 8 Ω	720 mW	THD+N = 10%, VDD = 3.6 V, RL = 8 Ω	750 mW
	THD+N = 1%, VDD = 4.2 V, RL = 8 Ω	1 W	THD+N = 1%, VDD = 5 V, RL = 8 Ω	1.4 W
	THD+N = 1% , VDD = 3.3 V, RL = 8 Ω	600 mW	THD+N = 1% , VDD = 3.6 V, RL = 8 Ω	630 mW

- Although MT6326 class-D power output is 1W at 8 Ω , because congenital power source limitation is 4.2V from VBAT , but compare with other discrete amplifiers , MT6326 equal other amplifier in performance.



TI Poutput Profile

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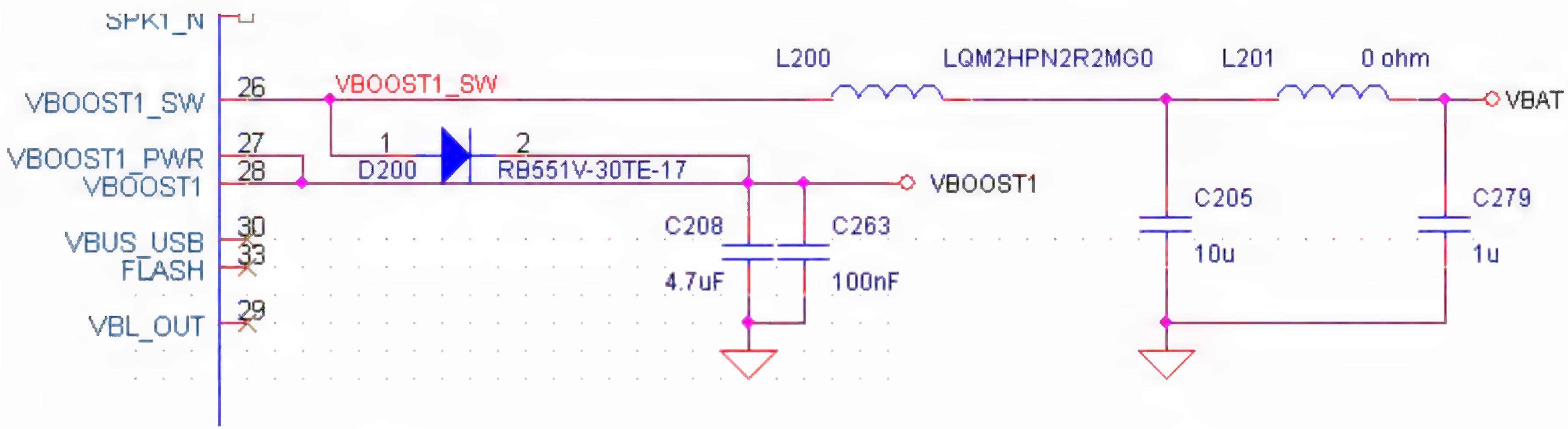
Boost1 For Parallel Backlight LCM or other 5V requirement



- Reserve filter at input/output to prevent interference to RF performance.
- L200/L201/C205/C279 should be in shield case and close near MT6326

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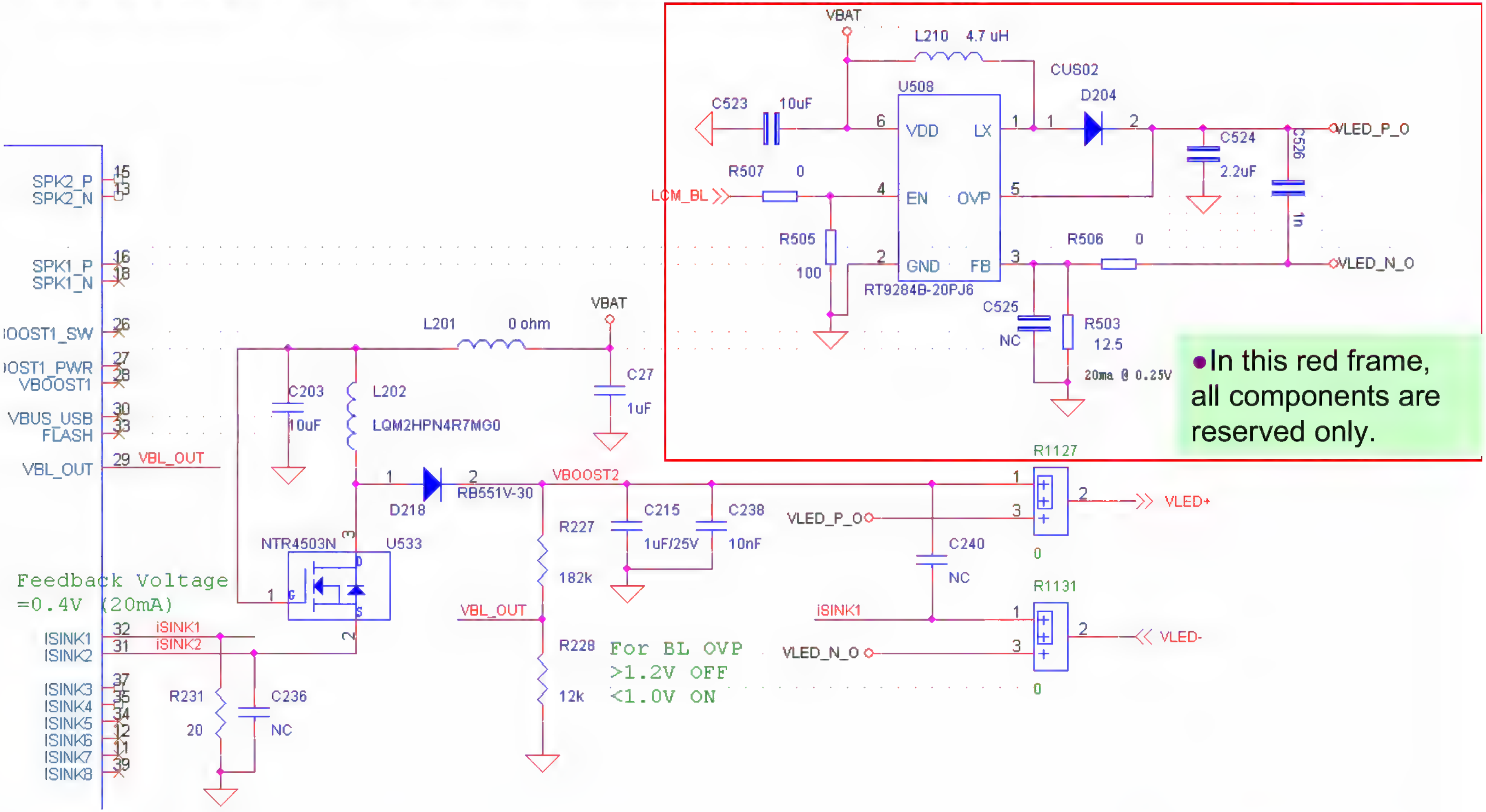
Boost2 For Serial Backlight LCM



- Reserve discrete B/L driver to prevent any improper design causing interference to RF performance.

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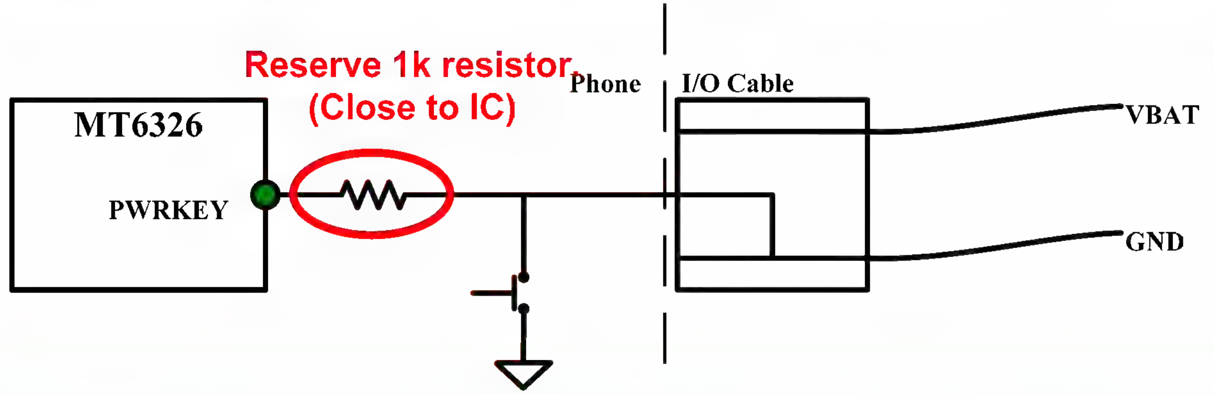
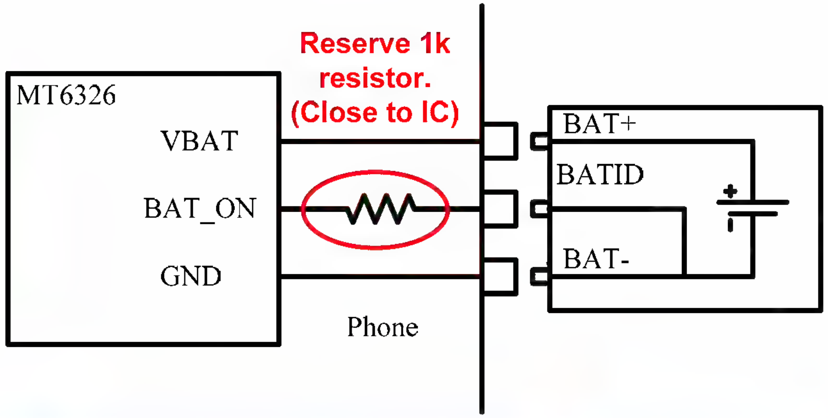
IC Protection: PWRKEY and BAT_ON



Please reserve 1k resistor on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

Please reserve 1k resistor on phone PCB to protect **BAT_ON** pin if BAT_ON is used to detect battery.



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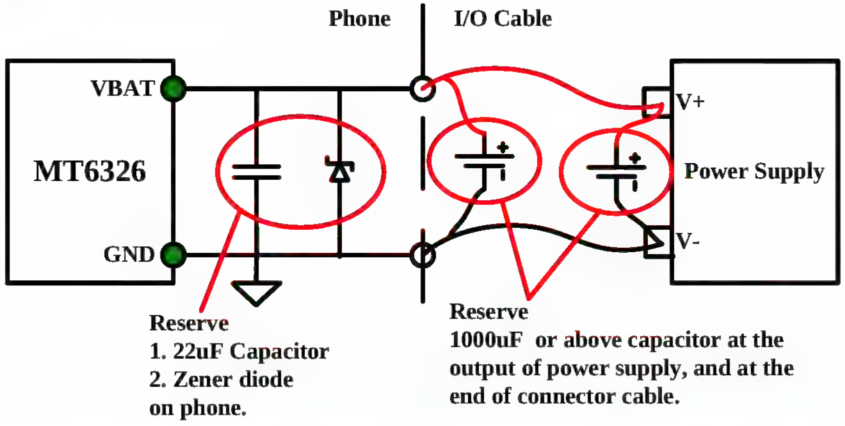
IC Protection: VBAT



MT6326 has lower VBAT voltage rating. (Max. 4.3V.) Some protection should reserve to prevent the damage by voltage surge.

•Design notice in Phone side:
1. At least 22uF capacitor.
2. Add Zener diode (5.1V) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6326.
Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.
Notice: Using 5.1V zener will introduce some leakage when VBAT = 4.2V.
•Design notice in Power Supply side:
Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible. Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

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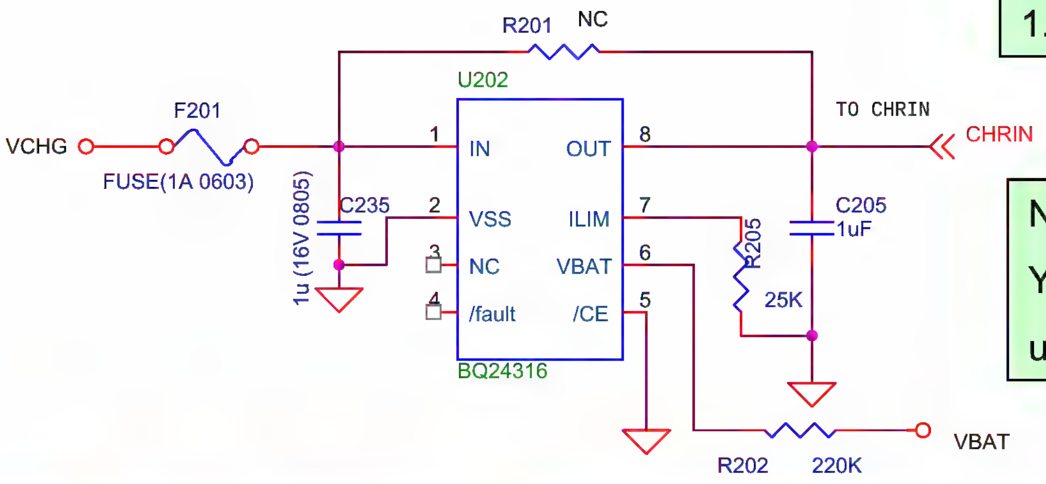
IC Protection: CHRIN

	MT6305 /MT6318	MT6223/35/38 /MT6326	External OVP/OCP
Max. Charger Input	15V	9V	30V
Charger OVP Point	9V	7V	6.8V

External OVP/OCP:



OVP/OCP Qualified Vendor :

1. TI – BQ24314

Notice :

You can get better charger protection by using external OVP/OCP device.

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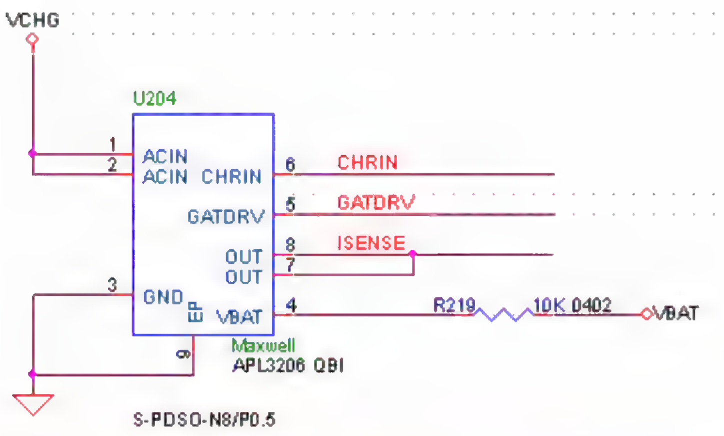
IC Protection: OVP + Charger

	MT6305 /MT6318	MT6223/35/38 /MT6326	External OVP/OCP
Max. Charger Input	15V	9V	30V
Charger OVP Point	9V	7V	6.17V(APL3206) 6.8V(APL3206A)

External OVP + Charger :



OVP/OCP + Charger Qualified Vendor :

1. ANPEC - APL3206 QBI

Notice :

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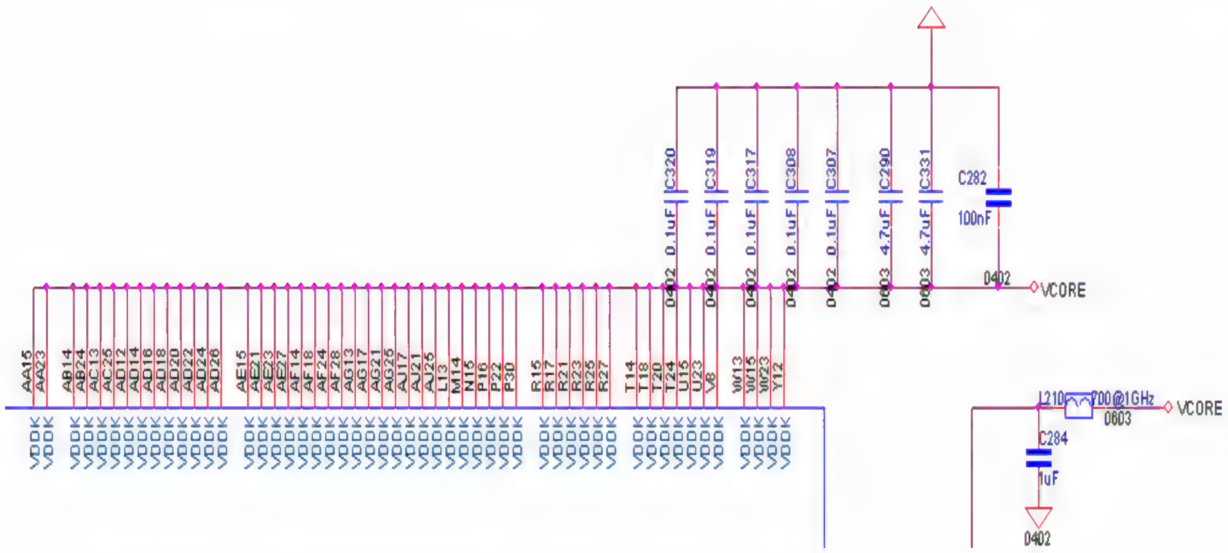
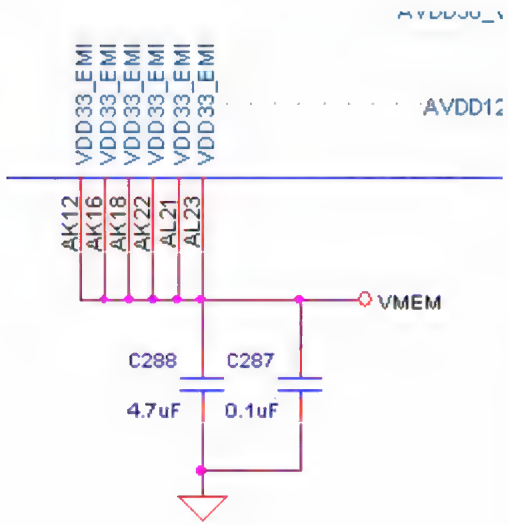
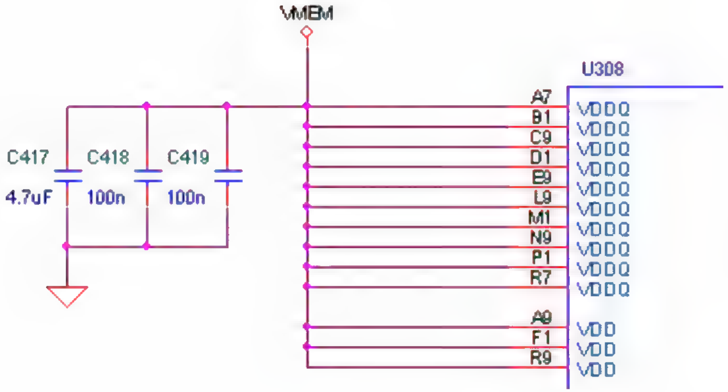
Bypass Capacitor: Vcore and VM





- Reserve enough bypass capacitors both at Vcore and VM to obtain good system stability.



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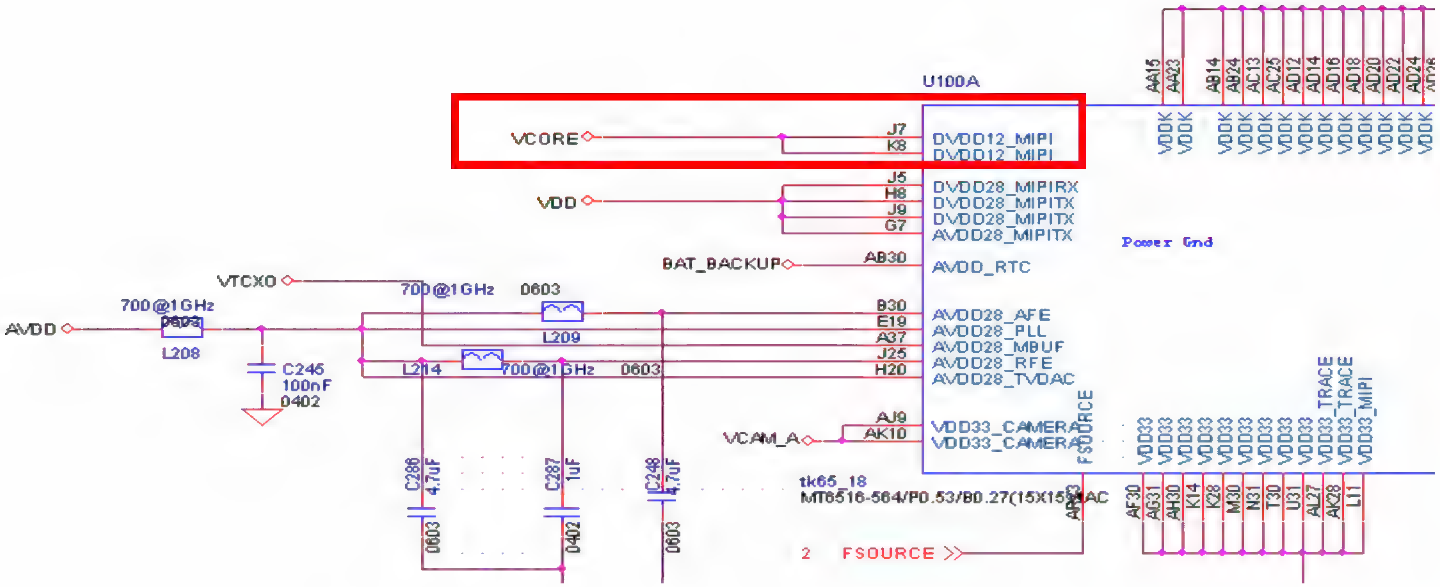
DVDD12_MIPI Power Connection



- MT6326 Vcore1 default is 1.3V , and MIPI_1.2V power spec. is 1.1~1.3V , so if need to use MIPI could connect Vcore2(if not used). Besides , must add external LDO for MIPI_1.2V.

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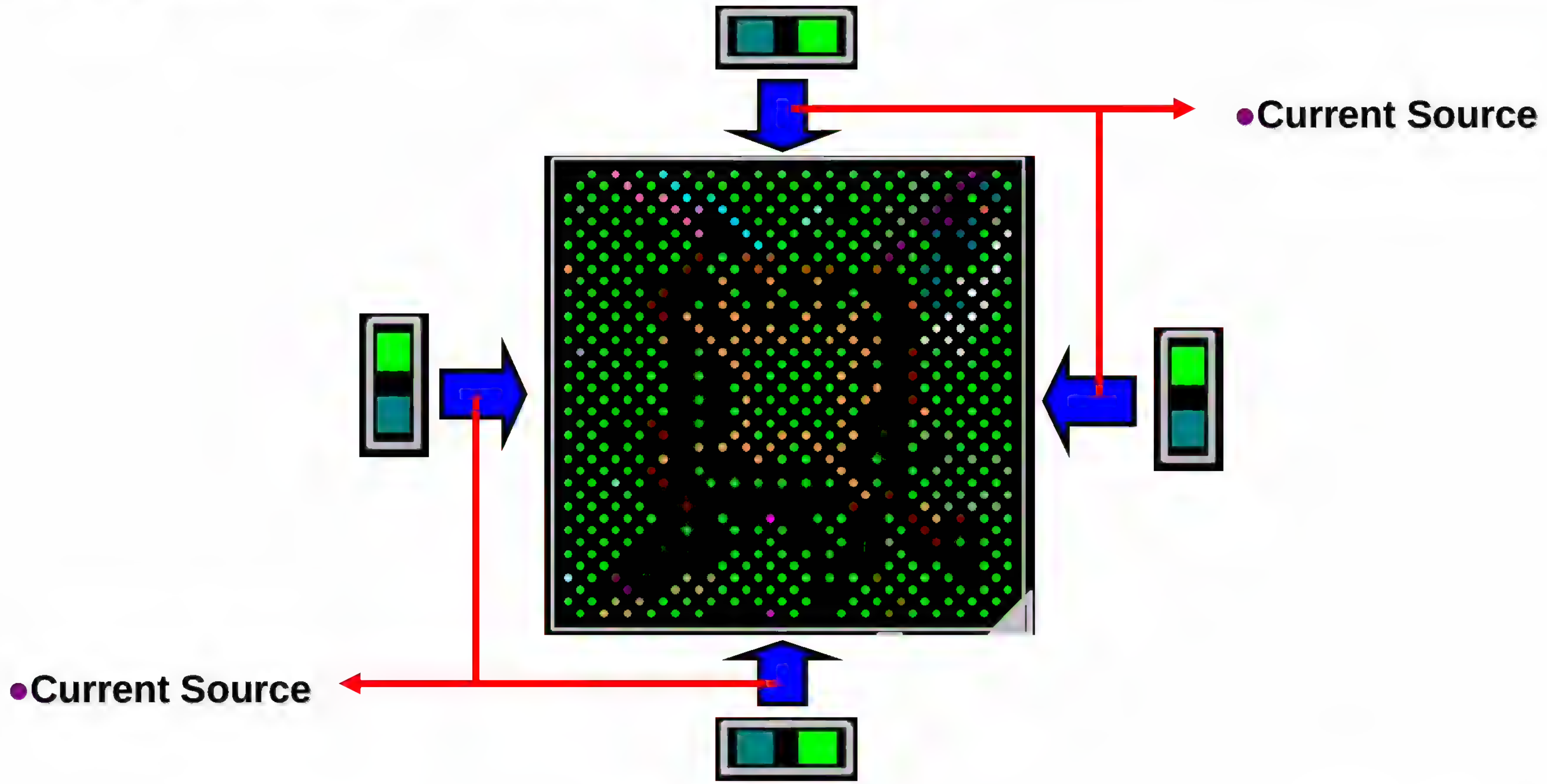
Bypass Capacitor: Layout Rule For Vcore



- Due to MT6516 have many Vcore (VDDK) balls , and these balls scatter around package of MT6516. Please put bypass capacitor around MT6516 to increase system reliably.

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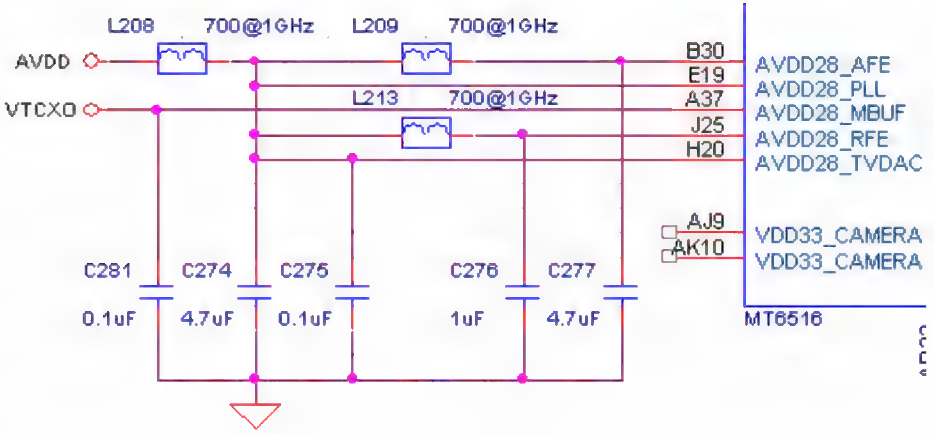
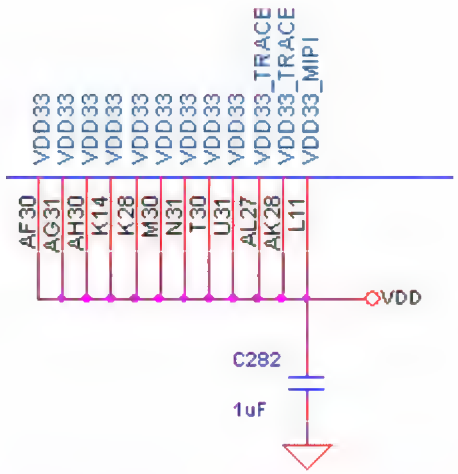
Bypass Capacitor: AVDD and VDD





- Reserve required input filter for ABB as specified in left schematics.
- AVDD28_MBUF suggest to connect to VTCXO.
- Reserve 1uF for I/O power input.

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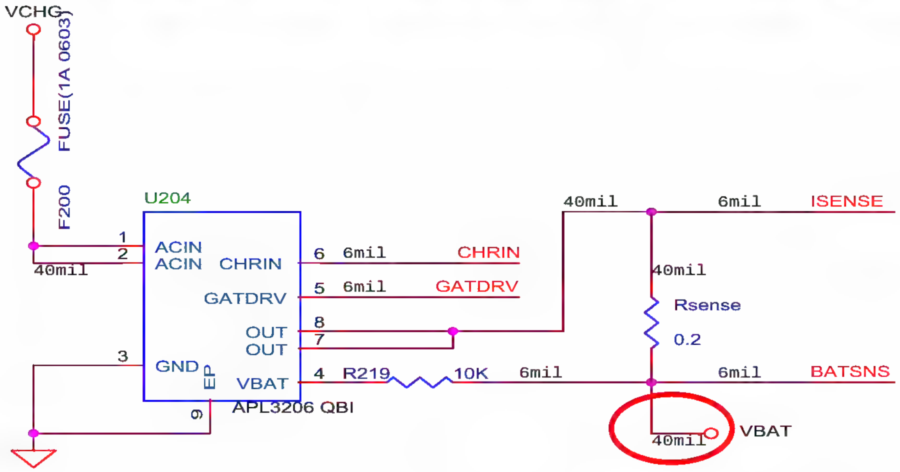
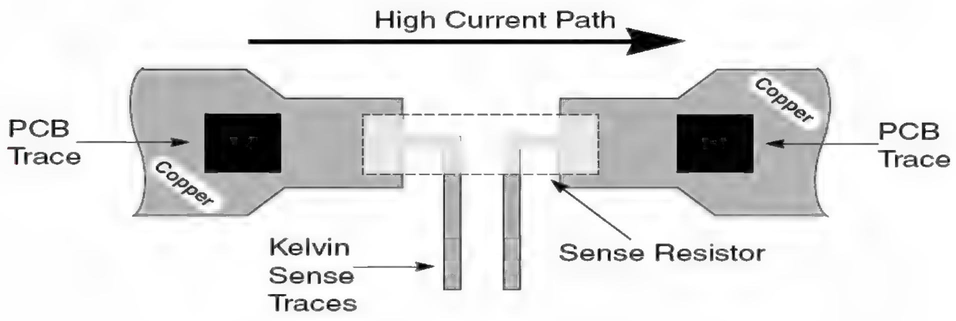
Layout Notice: Charging Path





- Charging related component (U204, Rsense, R219) should be close to battery connector.
- Minimum trace width are marked on the schematics above.
- ISENSE and BATSNS should be connected as the figure above.
- The trace from Rsense to battery connector (Marked in Red) should not share with other VBAT traces.
- ISENSE/BATSNS should be routed as differential traces which are away from noisy signals.

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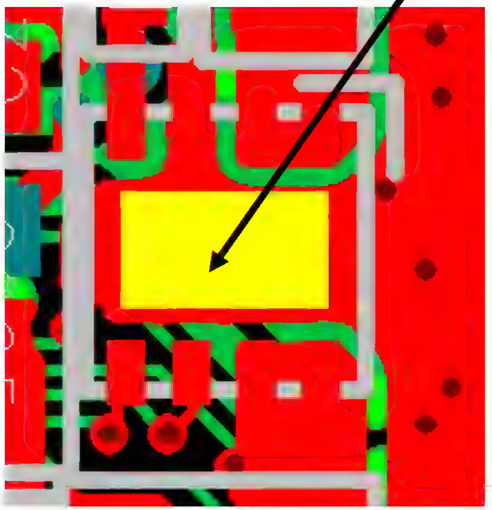
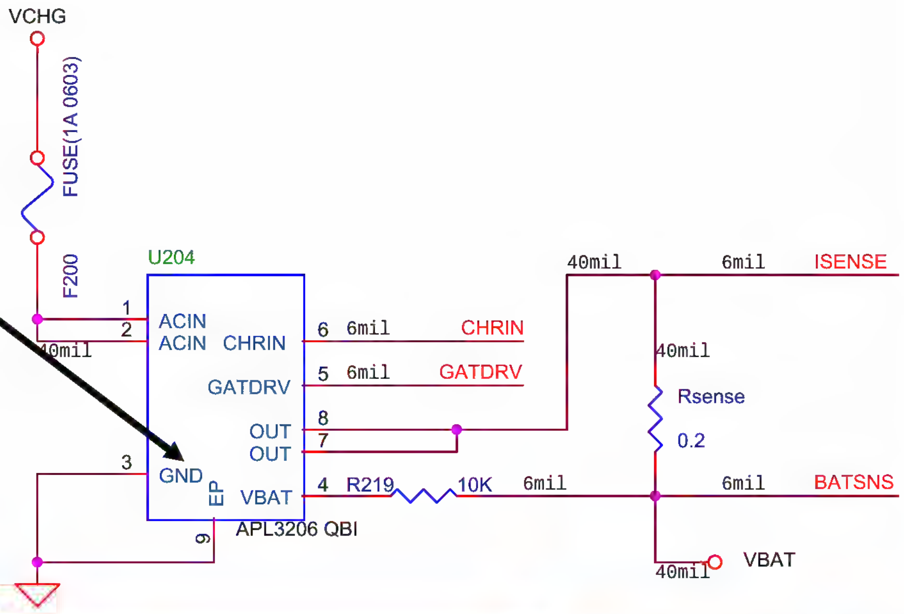
Layout Notice: Charger OVP IC

- The exposed pad of the charger OVP IC should connect to a large copper ground plane to get good thermal performance.
- The exposed pad should has at least 6 GND via connecting to inner layer.

Exposed pad to a large copper ground





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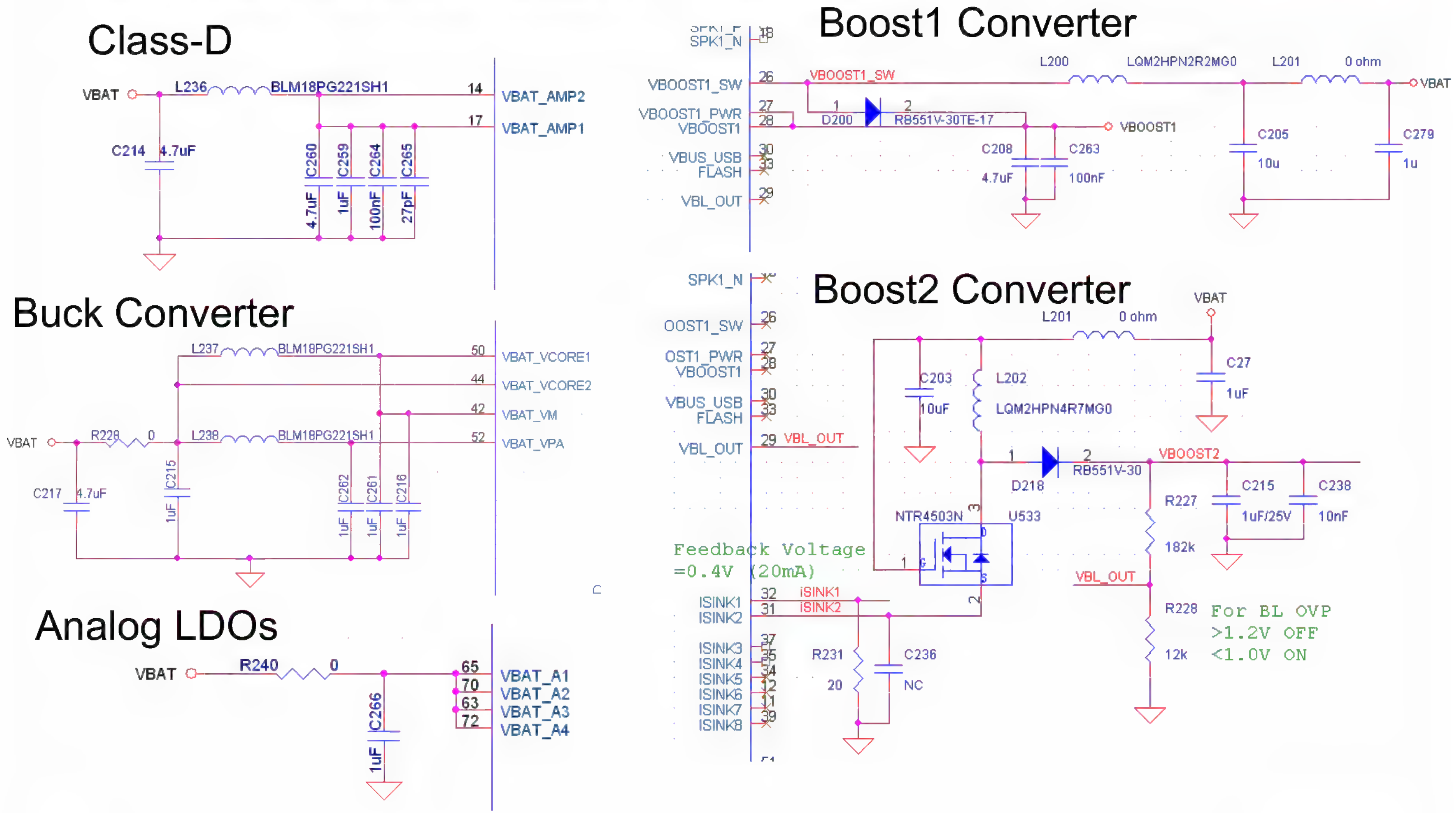
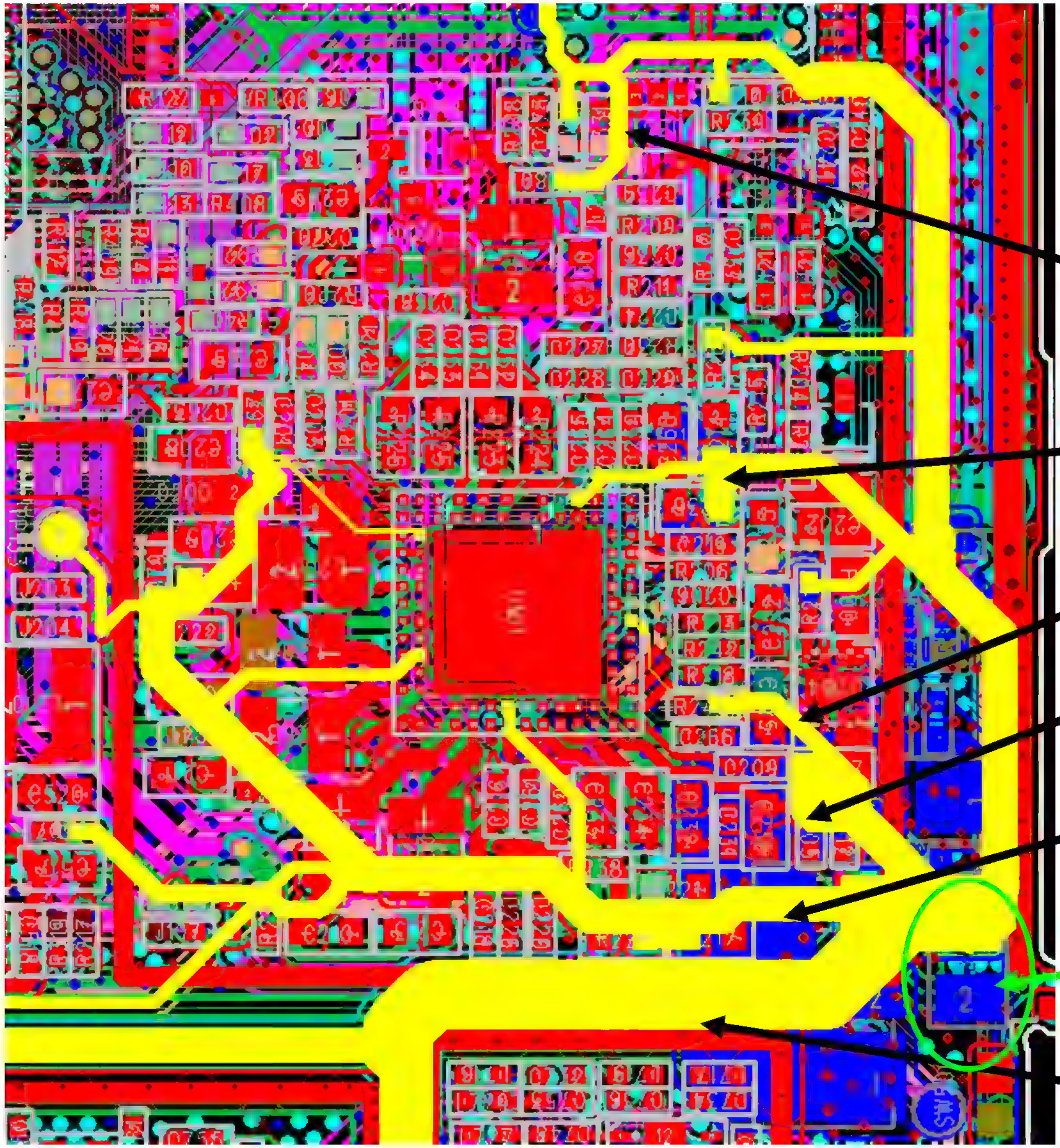
Layout Notice: VBAT Traces



- The VBAT for the 5 blocks show above (Class-D, Buck converter, Boost1, Boost2 converter and Analog LDOs) should star-connect to the bulk capacitor near battery connector.

Layout Notice: VBAT Traces

- Star-connect different VBAT group to BATTERY Connector directly



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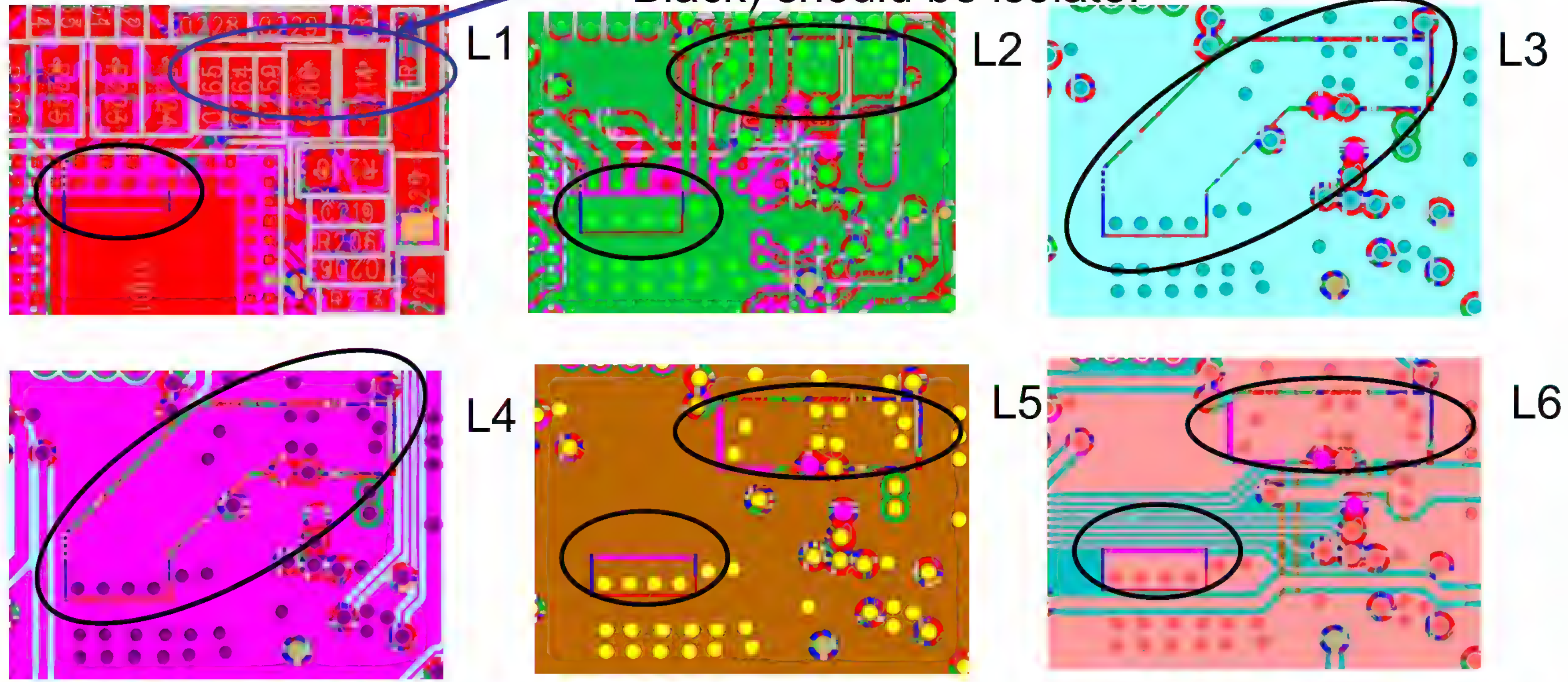
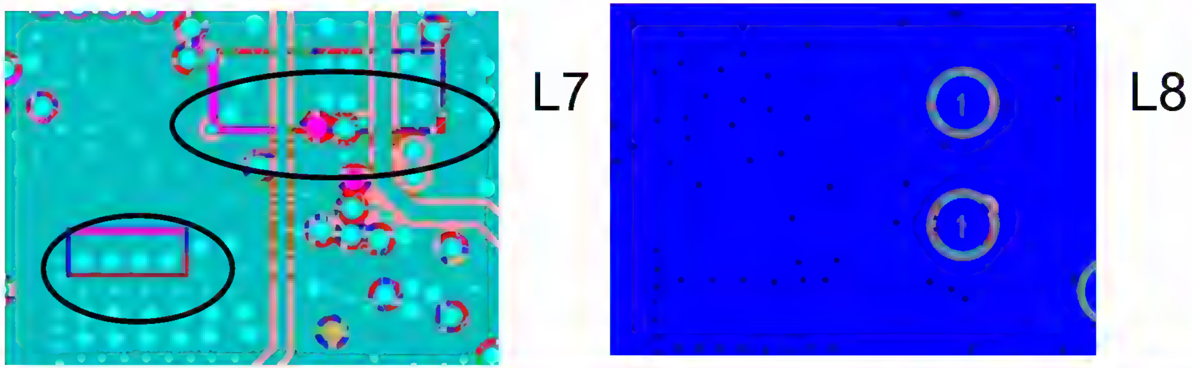
Class-D GND

GND merge, other GND (Mark by Black) should be isolate.





- The GND for Class-D should isolated carefully.

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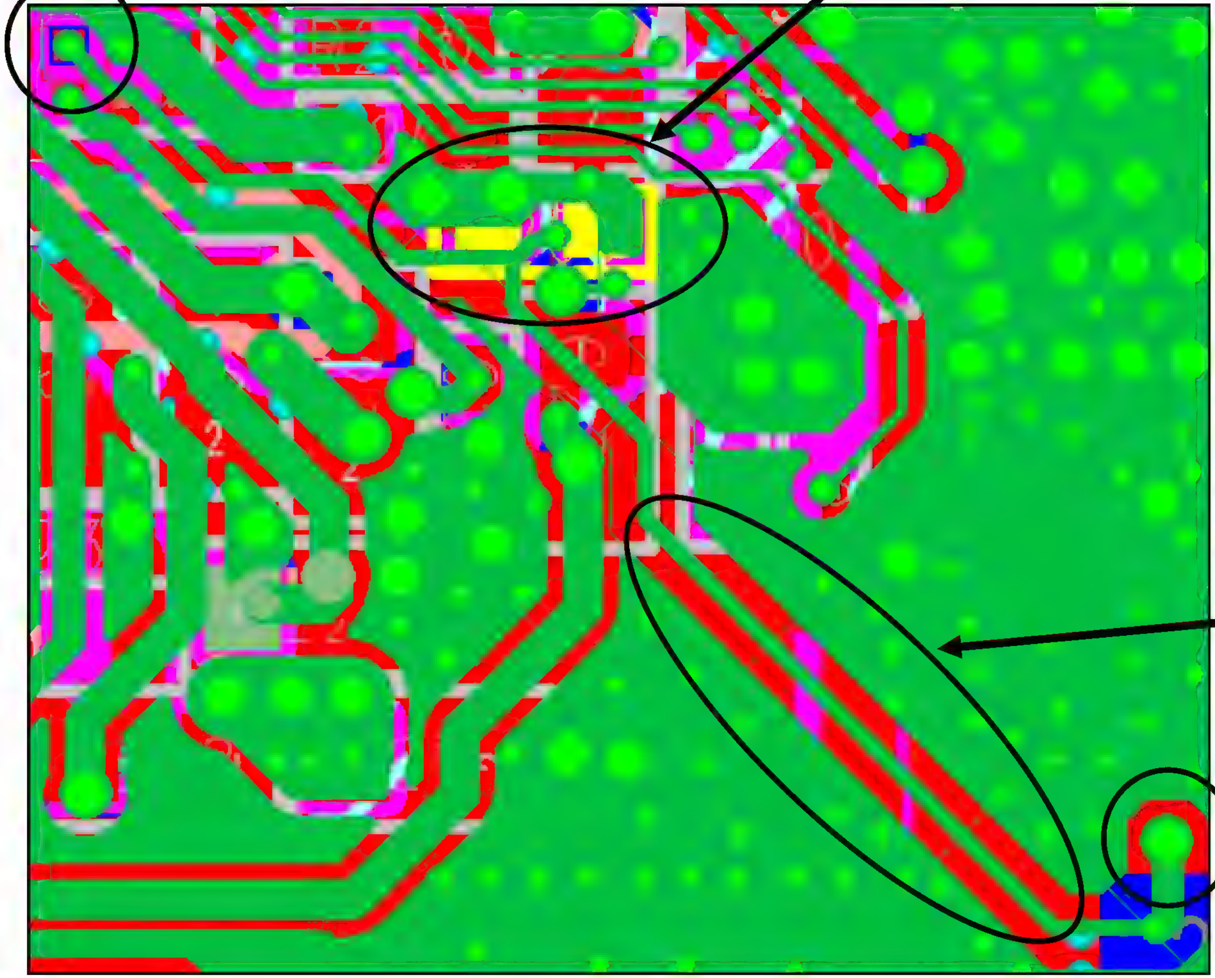
Layout Notice: GND_VREF Traces

Pin67 (GND_VREF)

Capacitor for VREF



- VREF capacitor (1uF) should be close to IC.
- GND_VREF (GND for VREF) should isolate carefully.

The trace should isolated and protected by GND

The trace should connect to GND of battery connector

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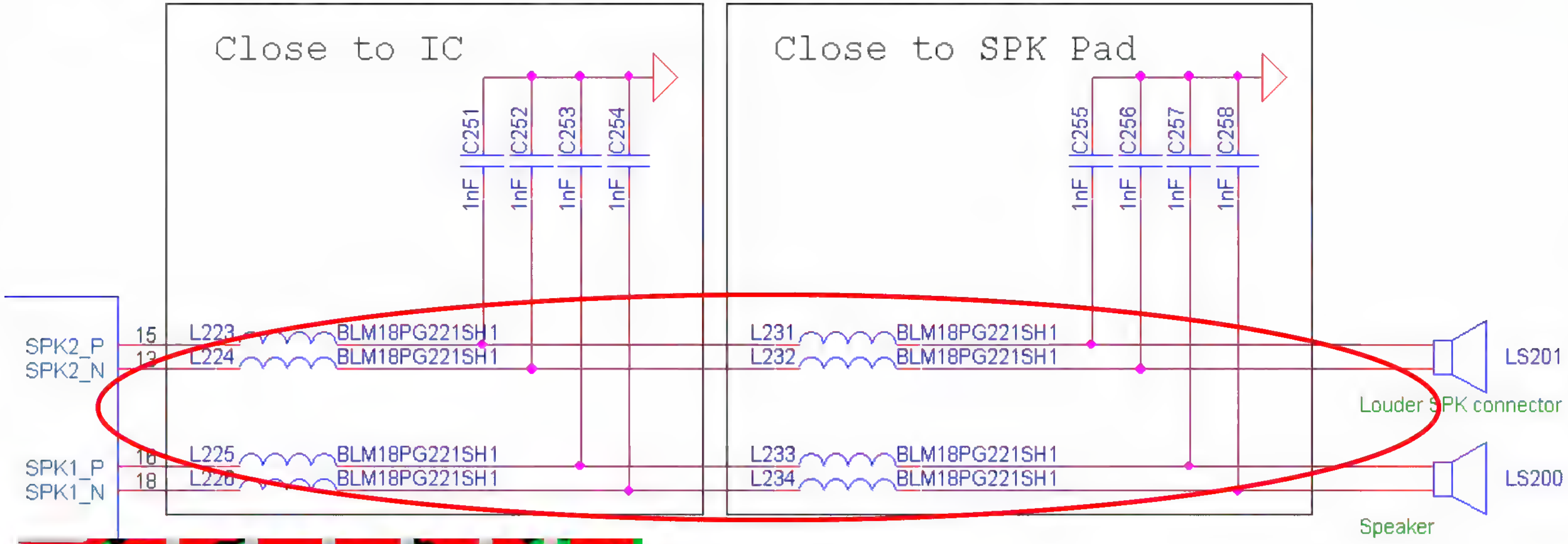
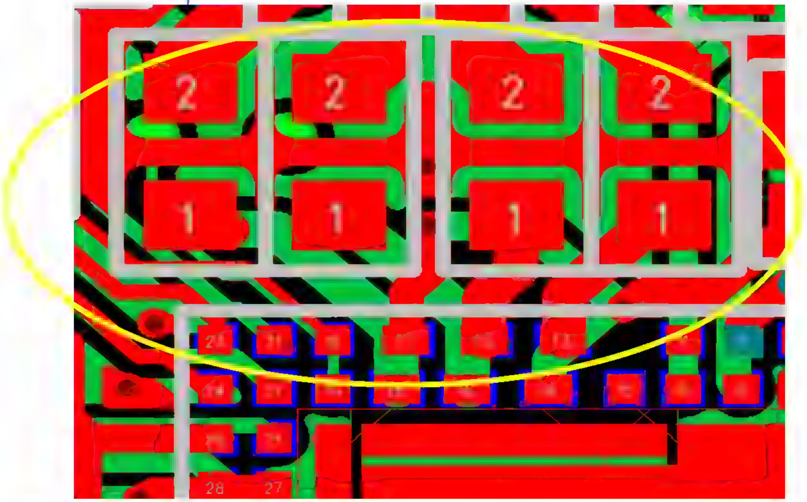
Layout Notice: Class-D Output





- The output trace (Marked in above schematics) should be differential, and protected by GND.
- 1st filter should be as close to IC as possible. (As the left figure showed.)
- The trace width should be
  - 8 ohm speaker: 25 mil.
  - 4 ohm speaker: 40 mil.

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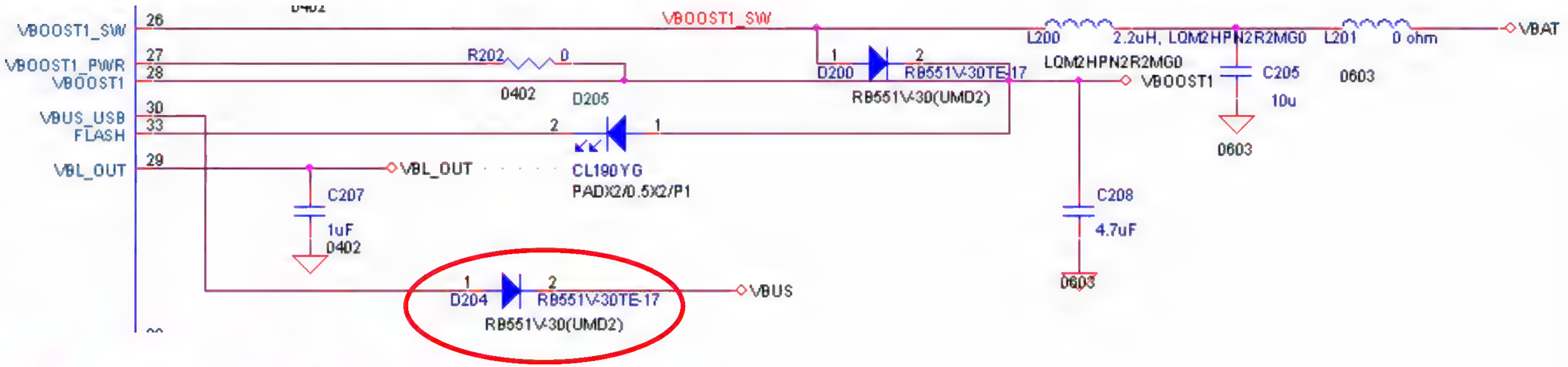
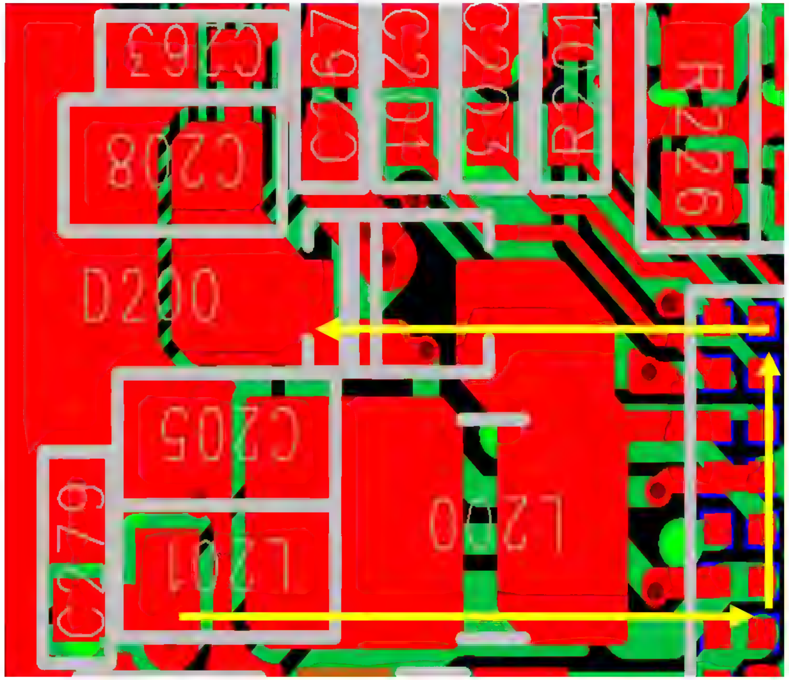
Layout Notice: Boost1





- Components should be as close to IC as possible.
- L200/D200/L201/C205/D200/C208 should be close and parallel to each other.
- The direction of L200/D200 should arrange as the arrowhead in left figure.
- Must add D204 to prevent feedback of VBUS when turn off boost1.

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MT6516 Design Notice (Audio)

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Outline

- Analog gain setting
- RC value
- PCB layout
- Audio feature
  - MP3 decoder
  - 3D surround effect
  - EQ 2.0
  - Audio AGC
  - Audio Compensation Filter

- For audio features, please refer to
  - L1_Audio_Design_and_Interface.pdf
  - Audio_Post-Processing_Interface_V1.13.pdf
  - Audio Customization v1.0.pdf

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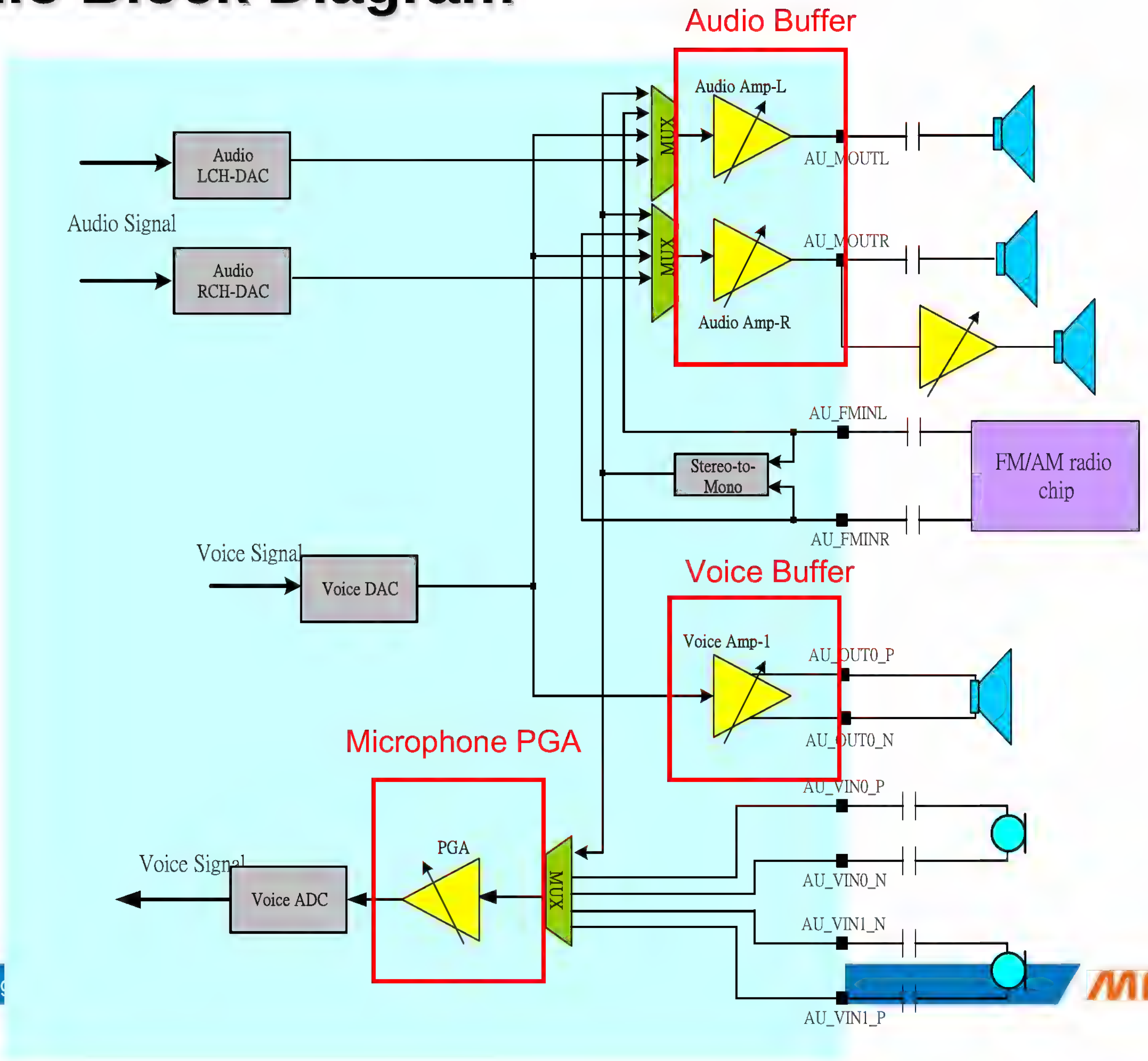
Audio Block Diagram



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Audio Buffer Gain

- Analog gain setting
  - **LoudSPK mode**
    - **Audio buffer**
      - 112= -1dB
      - Positive gain results distortion
    - **External amplifier**
      - increasing external amplifier gain for louder volume
  - **Earphone mode**
    - **Audio buffer**
      - 112= -1dB
      - Positive gain results distortion
    - **External RC trade-off**

setting in engineering mode	audio Buffer [dB]	voice Buffer [dB]
240	23	8
224	20	6
208	17	4
192	14	2
176	11	0
160	8	-2
144	5	-4
128	2	-6
112	-1	-8
96	-4	-10
80	-7	-12
64	-10	-14
48	-13	-16
32	-16	-18
16	-19	-20
0	-22	-22

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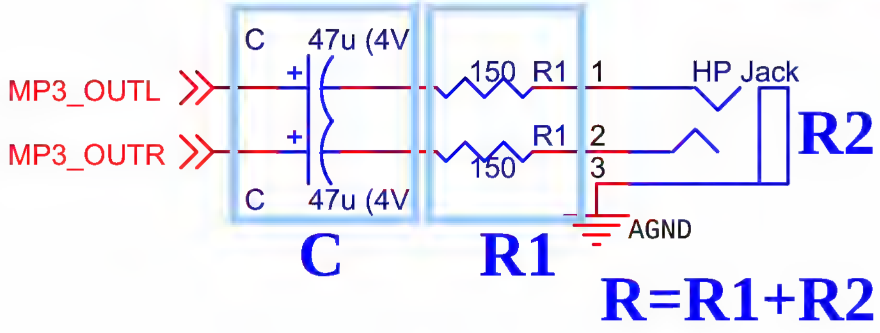
External RC value



- RC value on mp3_out path
  1) Bandwidth: $f_c = \frac{1}{2\pi RC}$
  2) Amplitude degradation: $amplitude\ [dB] = 20 \log \frac{R2}{R1 + R2}$
  3) Larger resistance, better bass, smaller volume;
  4) Larger capacitance, better bass, higher cost, larger PCB area.
  5) Pout < Earphone speaker rated power $P_{out} = \frac{(V_{rms})^2}{R2}$
  6) example:
     - (R1, C, Fc, Amplitude)
       - (100ohm, 47uF, 25.65Hz, -12.3dB)

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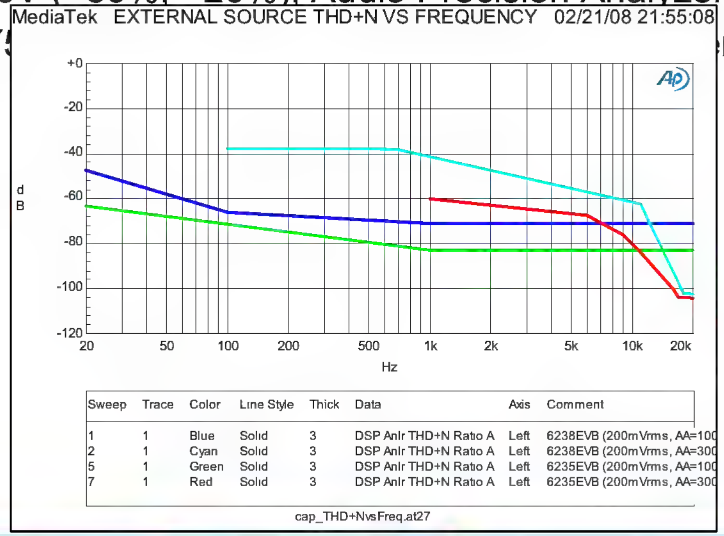
External RC value

- **Different types of capacitors have different distortion.**
  - distortion: Tantalum cap. > MLCC X5R > MLCC Y5V
  - Don't use MLCC Y5V in audio path/ mic0/ FM_IN
    - Capacitors' THD+N vs. Frequency are showed as below:
    - green: X5R (+/-10%); Audio Precision Analyzer Rin=100kohm
    - red: X5R (+/-10%); Audio Precision Analyzer Rin=100kphm
    - blue: Y5V (+80%, -20%); Audio Precision Analyzer Rin=300ohm
    - cyan: Y5 r Rin=300ohm



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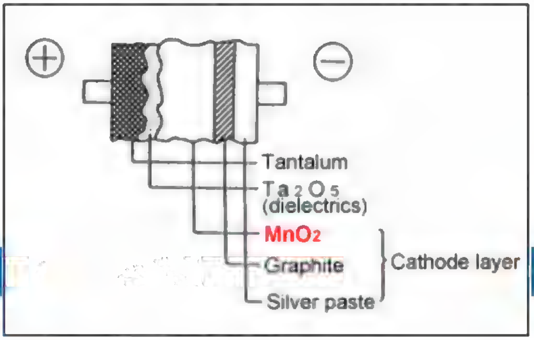
External RC value

- Tantalum capacitor
  - Can’t be operated under reverse bias,
    - HP EINT can’t be on earphone path.
  - Permissible reverse voltage:

<table>
<tr><td>Ambient Temperature</td><td>25°C</td><td>55°C</td><td>85°C</td><td>125°C</td></tr>
<tr><td rowspan="2">Permissible Reverse Voltage</td><td>R.V. × 10%</td><td>R.V. × 6%</td><td>R.V. × 3%</td><td rowspan="2">R.V. × 1%</td></tr>
<tr><td colspan="3">or 0.5V whichever is greater.</td></tr>
</table>

  - The reason of damage by reverse voltage
    - Reverse voltage will damage Ta2O5,
    - After Ta2O5 is broken, there is large current passed through tantalum capacitor.



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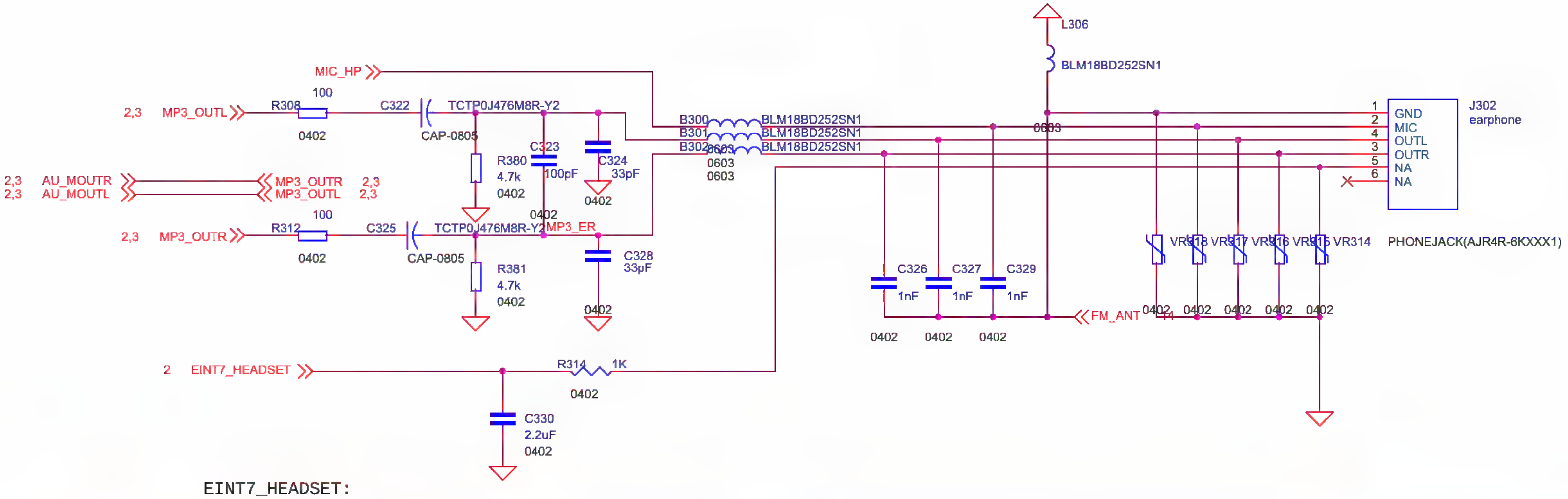
External RC value

- HP EINT suggestion
  - 18-pin I/O
    - An extra pin for HP EINT and accessory need a pull-low resister.
  - 6-pin earphone jack
    - Two extra pull-low resistors on CH-L/R



```
EINT7_HEADSET:
H= earphone plug in
L= earphone plug out
```

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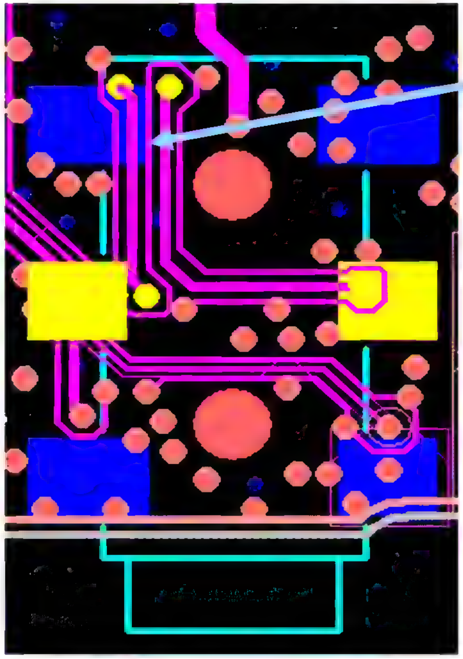
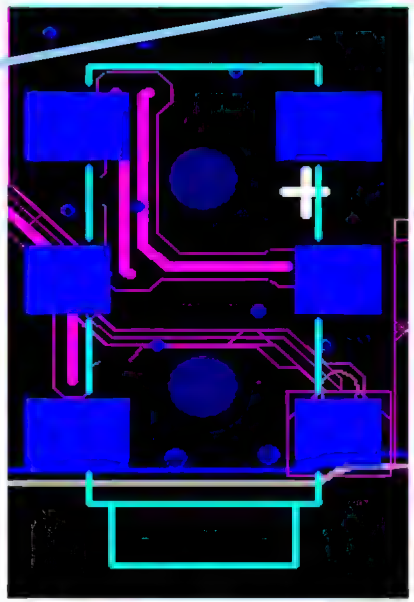
Audio Traces

- Crosstalk issue
  - avoid CH-L and CH-R’s signal interfering to each other
  - (1) PCB layout
    - **protected audio R & L stereo trace by GND separately.**



Crosstalk=70dB

Superman29_V2



Crosstalk=45dB

Superman29_V1

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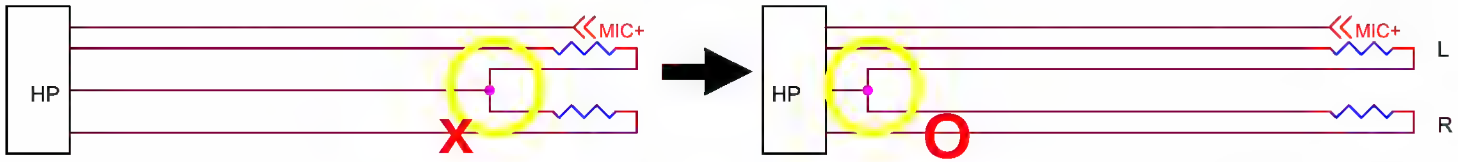
In headset mode, please separate L/R channel and microphone trace by GND.

Audio Traces

- Crosstalk issue
  - (2) earphone accessory:
    - Separated GND of CH-L and CH-R.
    - connect the GND of CH-L and CH-R at the end of earphone jack. Not connect the GND at earphone microphone.



  - (3) The bead at FM ANT on earphone path may degrade crosstalk about 15dB.
    - Choose bead with low DRC bead and good THD+N
    - It is a trade-off between FM feature and crosstalk performance.

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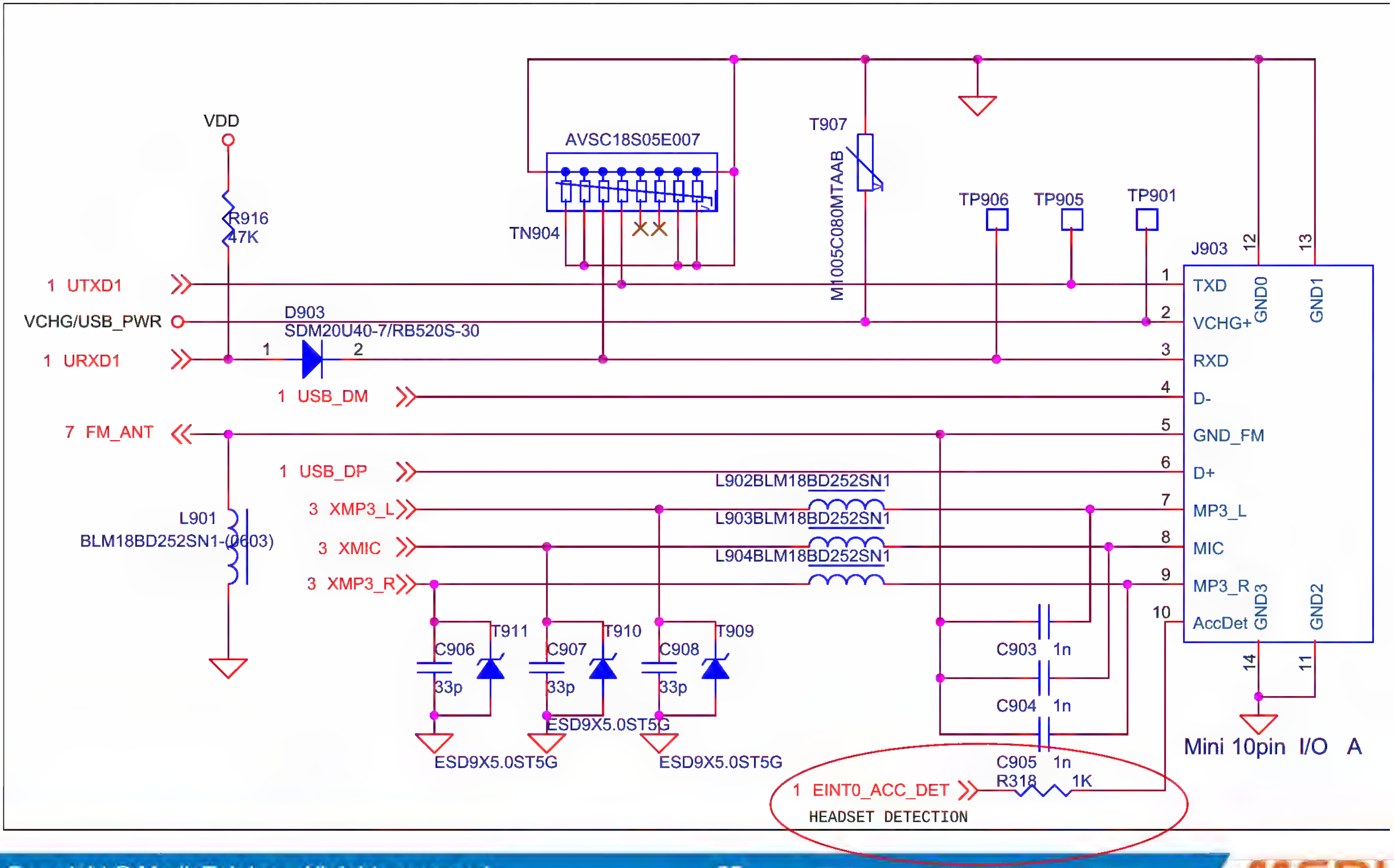
I/O connector (10pins)

- UART + USB + Earphone



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Case Study (1)

- **Audio pop noise**
  - LoudSPK mode
    - Tuning external audio amplifier ON/OFF delay time
    - mp3_outL/R to external amplifier input must add coupling capacitor to avoid voltage drop.
  - Earphone mode
    - Turn on de-pop function by software
    - Tantalum capacitor +/- reverse mounting.

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Case Study (2)

- **Loudness without distortion**
  - LoudSPK mode
    - Audio buffer gain <112
    - Increase external audio amplifier gain
  - Earphone mode
    - Audio buffer gain <112
    - decrease resistance on earphone path
      - Increase capacitance for good bandwidth
  - Microphone PGA
    - **uplink speech volume**
      - nvram_default_audio.c: #define GAIN_NOR_MIC_VOL3
      - Engineering mode: audio, normal mode. microphone, volume3
    - **sound recorder/video recording volume**
      - nvram_default_audio.c: #define GAIN_NOR_MIC_VOL4
      - Engineering mode: audio, normal mode. microphone, volume4
    - **FM recorded file playback**
      - Increase FM_record_PGA if FM playback volume is small.
      - mcu\1audio\afe2.c: #define FM_RADIO_RECORDING_VOLUME

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MT6516 Design Notice (Speech)

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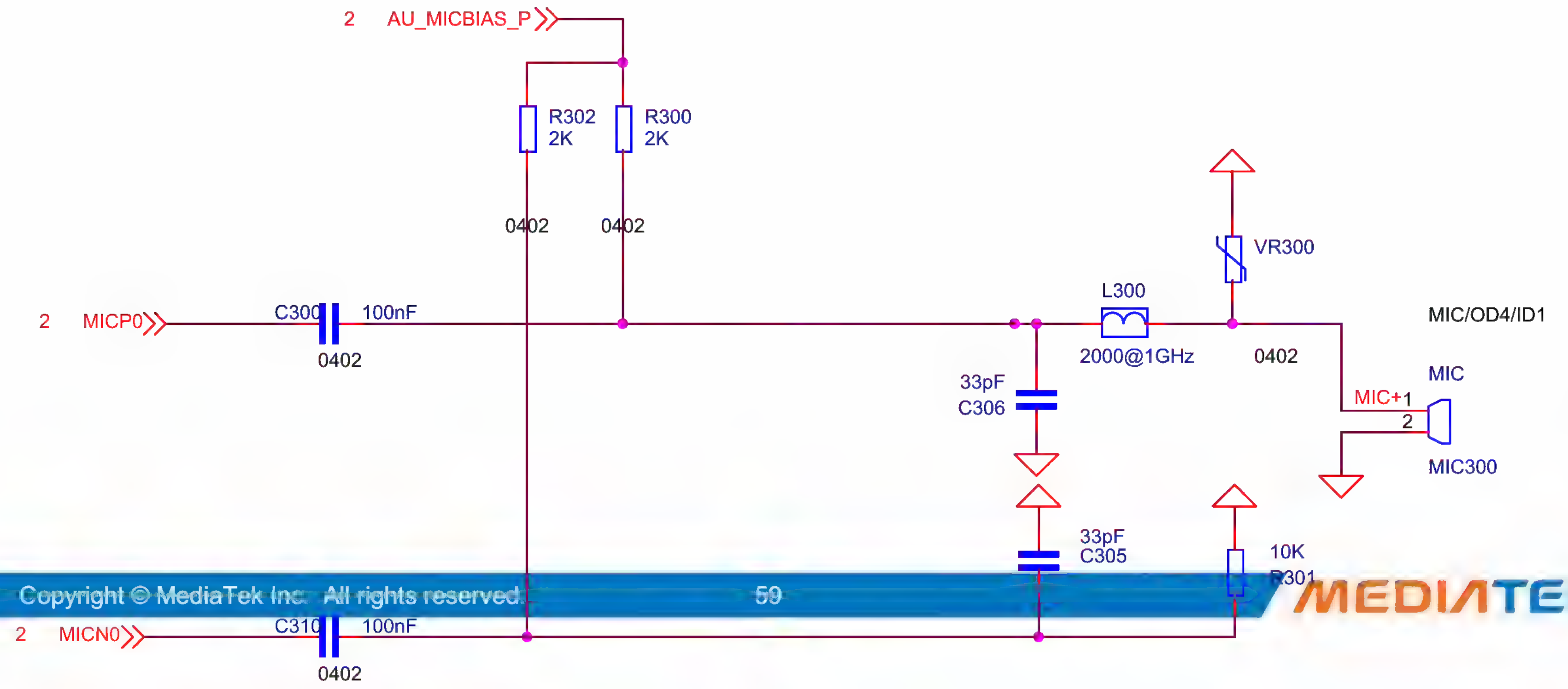
New Proposed Microphone Circuit

- Advantage
  - 10uf capacitor is not needed any more
  - Less passive components are needed
- Circuit: Normal mode



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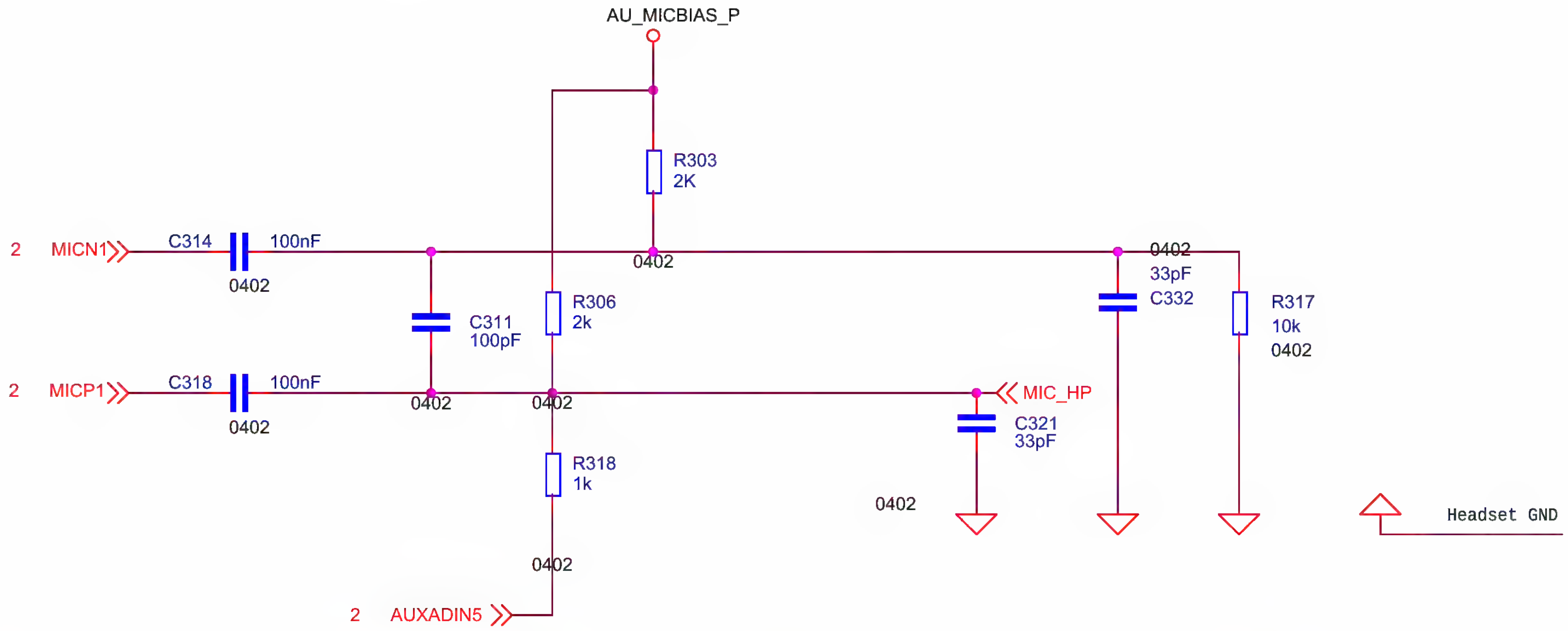
New Proposed Microphone Circuit

- Circuit: Headset mode



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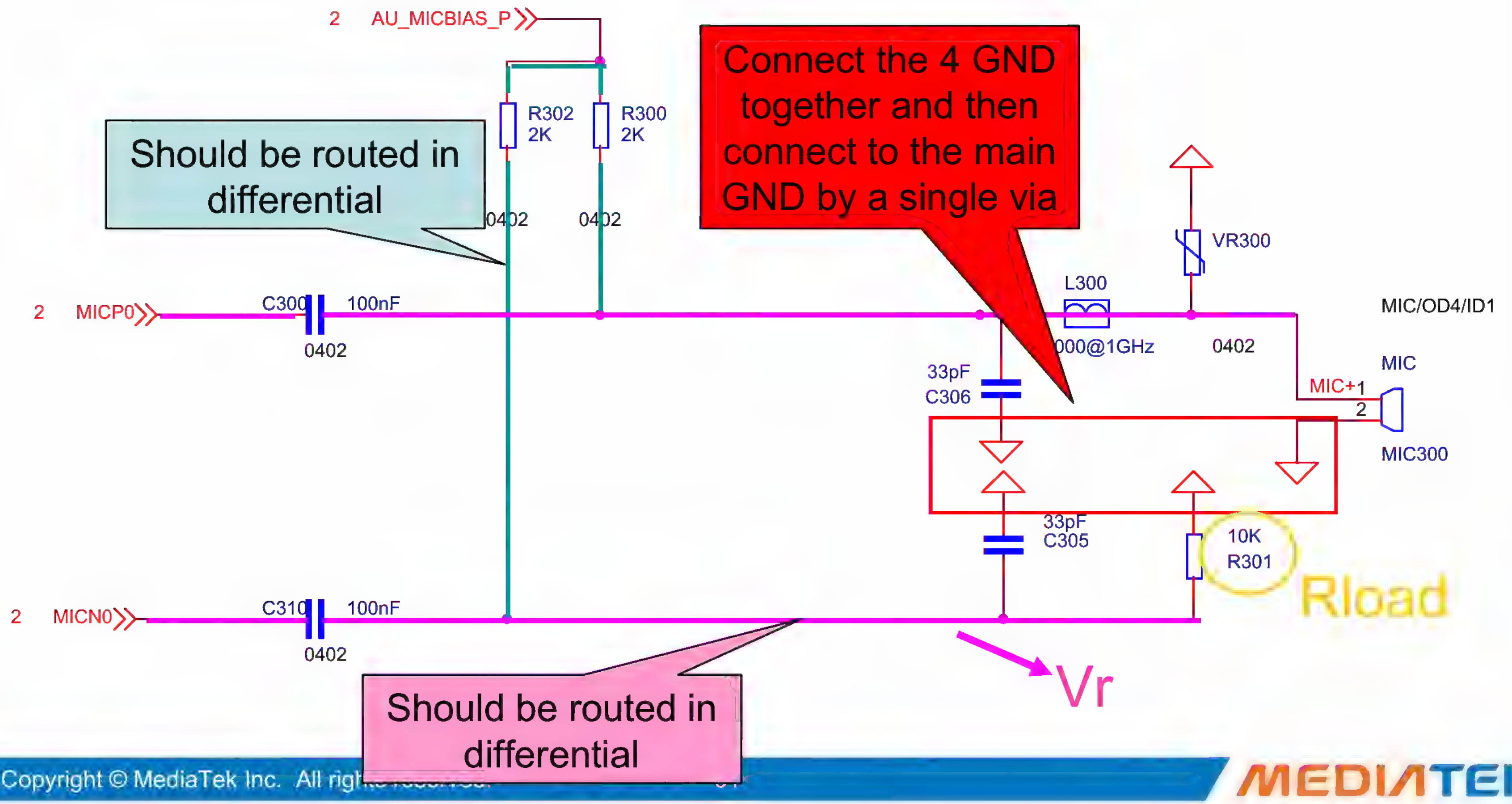
New Proposed Microphone Circuit

- Layout consideration-Normal mode



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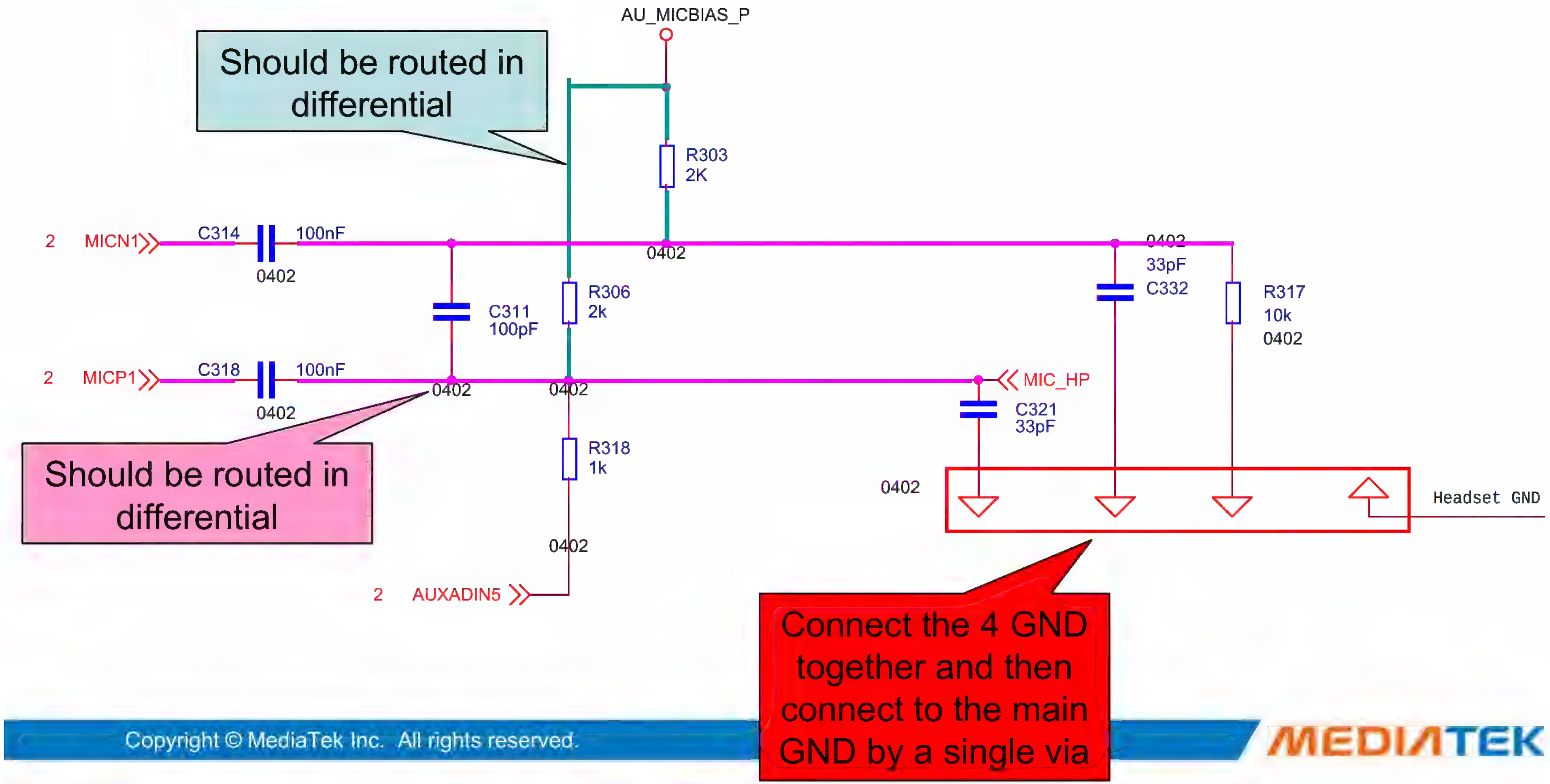
New Proposed Microphone Circuit

- Layout consideration-Headset mode



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How to Optimized Rload

- The Rload can be calculated by the follow procedure
  - Measure the voltage on the microphone MIC_P in a quite environment
  - Select a Rload to let Vr has almost the same voltage as MIC_P

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MT6516 Camera Design Notice

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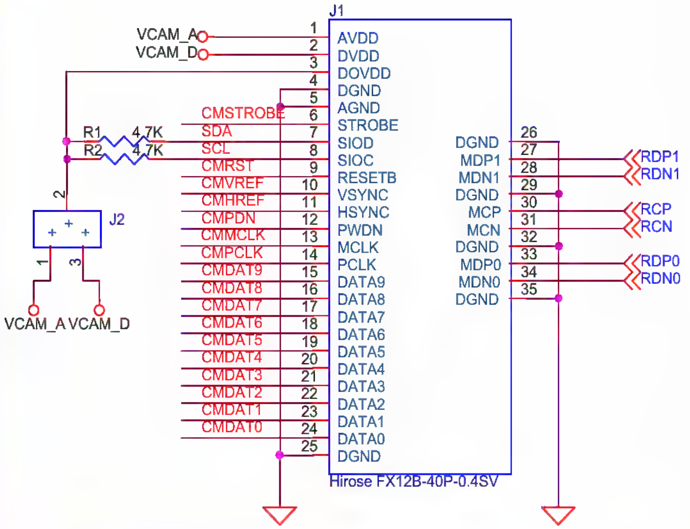
Camera Design Note – Parallel Interface

- All camera pins are dedicated
- Layout notice
  - CMMCLK, CMPCLK need to be well shielded by GND plane
- BB side power level
  - VDD33_CAMERA (AJ9, AK10) = Camera side IO level DOVDD

MT6516 (Pin definition)		Camera side
CMVREF	AH8	VSYNC
CMHREF	AT2	HSYNC
CMPCLK	AG9	PCLK
CMMCLK	AR3	MCLK
SDA1	AP2	SIOD
SCL1	AG5	SIOC
CMRST	AJ7	RESETB
CMPDN	AM4	PWDN
CMDAT0~CMDAT9	AV2,AL9,AT4,AM8,AU3 AN7,AN5,AK8,AP4,AL7	DATA0 ~ DATA9
CAM_STROBE	AN3	STROBE



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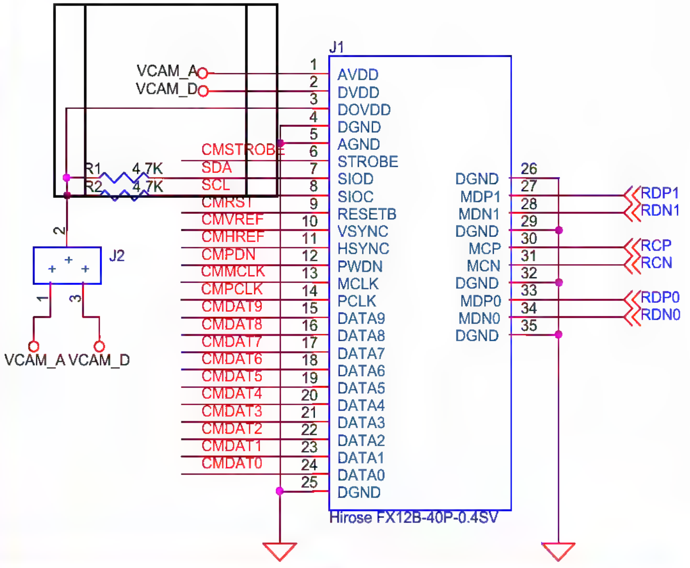
Camera Design Note – MIPI (CSI-2) Interface

- All MIPI DSI pins are dedicated that connect from BB to LCM
  - 1 CLK Lane + 2 Data Lanes
- BB side TVRT (pin G5) connect 1.8K 1% resistor to GND and close to BB
- Layout notice
  - All signal pairs need to 50ohm impedance matching for single end and 100ohm for differential
  - All signal length need be equal and well shielded by GND plane
- BB side power level
  - VDD33_CAMERA (AJ9, AK10) = Camera side IO level DOVDD
  - DVDD12_MIPI (J7, K8) connect to VCORE(1.2V)
  - DVDD28_MIPITX (H8, J9), DVDD28_MIPIRX(J5), AVDD28_MIPITX (G7), and VDD33_MIPI (L11) connect to VDD (2.8V)

MT6516 (Pin definition)		Camera side
RDP1	H2	MDP1
RDN1	G1	MDN1
RCP	G3	MCP
RCN	F2	MCN
RDP0	E3	MDP0
RDN0	E1	MDN0
CMRST	AJ7	RESETB
CMPDN	AM4	PWDN
CAM_STROBE	AN3	STROBE



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MT6516 LCM Design Notice

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Display Interfaces

- Various Interface Support
  - 8080 host IF (MIPI DBI)
  - 8/9/16/32-bit Serial IF
  - RGB interface (MIPI DPI)
  - MIPI DSI interface
- High performance LCD controller enable wide range of display resolution
  - Landscape or Portrait mode.
  - From 128x96(SubQCIF) ~ 852x480(WVGA)
- Advance color processing
  - Embedded LCD Gamma correction table.
  - Color correction matrix.
  - true color support.
  - Contrast, brightness adjustment.
  - 6 overlay layers with per-pixel alpha channel and gamma table
  - 2x or 4x temporal dithering

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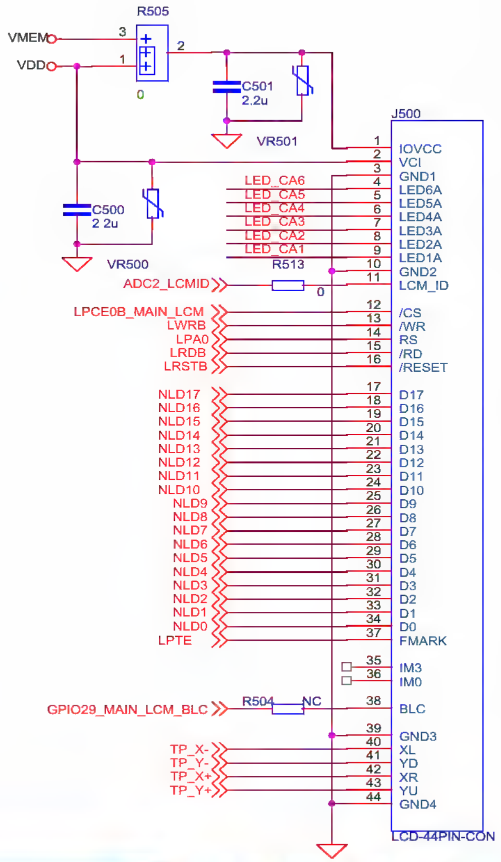
LCM Design Note – CPU (Host) Interface

- LCM side must have FMARK(F_Sync) frame update HW pin and need to connect to LPTE(W3) for tearing free Tier-1 performance
- LCM side IOVCC reserve VMEM(1.8V) & VDD(2.8V) option for 1.8V NAND application
- BB side power level
  - VDD33_NLD (pin AA9, AC9, W9) = LCM side IOVCC level

MT6516 (Pin definition)		LCM side
LPCE0B	W1	/CS
LWRB	AA1	/WR
LPA0	Y4	RS
LRDB	Y2	/RD
LRSTB	W7	/RESET
NLD17~NLD0	AA5, AF2, AP6, AE3, AB8, AD4, AC7, AJ1, AH2, AL1, AG3, AF4, AC5, AK2, AD6, AJ3, AD8, AN1	D17~D0
LPTE	W3	FMARK / F_Sync



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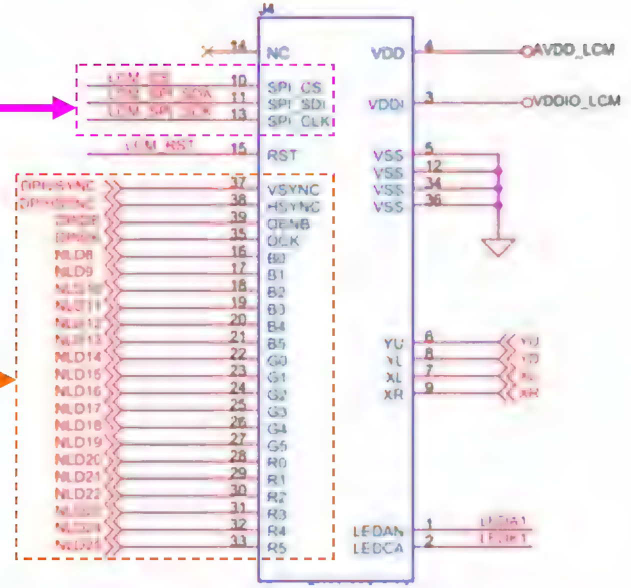
LCM Design Note – RGB (DPI) Interface

- RGB (DPI) interface separated into two groups
  - 3 wire (or 4 wire) SPI interface for LCM initial code setting
  - Image databus (Dedicated pins and connect from BB to LCM directly)
- Layout notice
  - DPICK, LSCK must well isolated by GND plane
  - All Image signal length need to be equal as best.
- BB side power level
  - VDD33_NLD (pin AA9, AC9, W9) = LCM side IOVCC(VDDI) level

MT6516 (Pin definition)		LCM side
LSCE0B	V4	SPI_CS
LSDA	U1	SPI_SDI
LSCK	U5	SPI_CLK
DPIVSYNC	AA3	VSYNC
DPIHSYNC	W5	HSYNC
DPIDE	AB2	DENB
DPICK	AC1	DCK
NLD8 ~ NLD13	AL1,AH2,AJ1,AC7,AD4,AB8	B0 ~ B5
NLD14 ~ NLD19	AE3,AB6,AF2,AA5,AG1,Y8	G0 ~ G5
NLD20 ~ NLD25	AC3,AA7,AD2,AE1,AB4,Y6	R0 ~ R5
LRSTB	W7	RST



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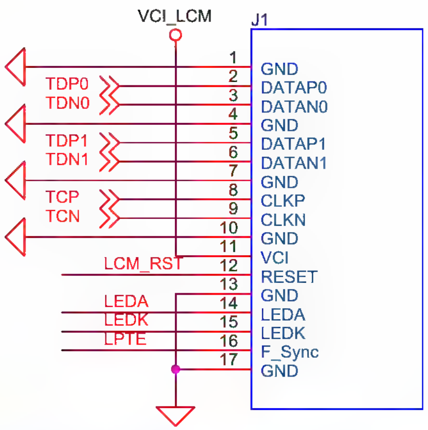
LCM Design Note – MIPI (DSI) Interface

- All MIPI DSI pins are dedicated that connect from BB to LCM
  - 1 CLK Lane + 2 Data Lanes
- F_Sync for MIPI DSI command mode connect to dedicated pin LPTE
- BB side TVRT (pin G5) connect 1.8K 1% resistor to GND and close to BB
- Layout notice
  - All signal pairs need to 50ohm impedance matching for single end and 100ohm for differential
  - All signal length need be equal and well shielded by GND plane
- BB side power level
  - VDD33_NLD (pin AA9, AC9, W9) = LCM side IOVCC(VDDI) level
  - DVDD12_MIPI (J7, K8) connect to VCORE(1.2V)
  - DVDD28_MIPITX (H8, J9), DVDD28_MIPIRX(J5), AVDD28_MIPITX (G7), and VDD33_MIPI (L11) connect to VDD (2.8V)

MT6516 (Pin definition)		LCM side
PAD_TDP0	C1	TDP0
PAD_TDN0	D2	TDN0
PAD_TDP1	A3	TDP1
PAD_TDN1	B4	TDN1
PAD_TCP	B2	TCP
PAD_TCN	C3	TCN
LRSTB	W7	RESET
LPTE	W3	F_Sync / TE



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High Speed Memory Layout Rule
Mobile DDR SDRAM

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Outline

- Overview
- High speed memory layout considerations
  - Placement
  - Suggested routing order
  - Ground/Power plane
  - Signal layout
  - Other general layout considerations
- Check list

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Overview

DDR SDRAM signals

- We can categorize DDR SDRAM interfaces into 4 groups as follows.
- Signal quality could be degraded by any PCB layout issue.
- We must take care of different groups of DDR SDRAM.

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask
Clock	CLK CLK#	Memory Differential Clock Memory Inverted Differential Clock
Command	A[0:15] BA[0:1] RAS CAS WE	Address Bus Bank Select Row Address Select Column Address Select Write Enable
Control	CKE CS	Clock Enable Chip Select

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High Speed Memory Layout Considerations

- It is recommended that the PCB layout of memory interface is the first priority for your design.
- We can check memory PCB layout characteristics in the following order:
  1. Placement
  2. Suggested routing order
  3. Ground/Power plane
  4. Signal layout
  5. Other general layout considerations

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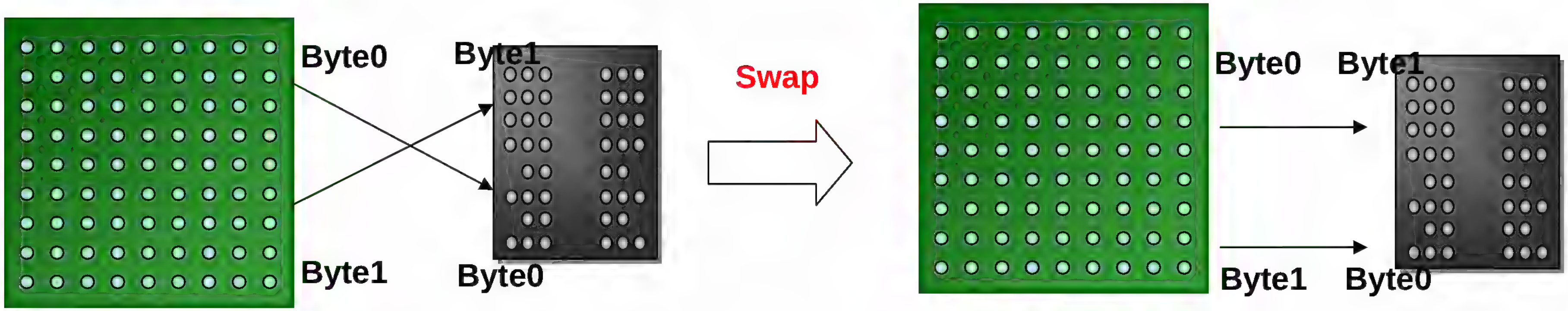
High Speed Memory Layout Considerations

- Placement
  - Memory device must place as close to BB Chip as possible
  - Avoiding extra long trace (Max trace1500mil)
  - Avoiding other high frequency devices place close to Memory
  - Route these traces smoothly, reduce the via counts and avoiding traces interlace if possible
  - You can swap byte in order to reduce traces interlace if there has restriction in placement (only for SD/DDR RAM)



  - “Swap byte” means to connect DQS0 from BB chip to memory DQS1 in order to reduce the interlacing of data traces, e.g. D[0:7] from BB chip to memory D[8:15].
  - Note: Swap the corresponding DQS ,DQM and DQx at the same time.

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High Speed Memory layout considerations

- Layout routing
  - Please route traces by the following order:
    1. Power/GND plane
    2. Data group
    3. Clock group
    4. Command/Address/control groups
  - Because high frequency signal integrity is highly related to solid ground and power plane, data groups are operating at twice the clock frequency.
  - It is recommended that the designer takes care of the layout routing in the very beginning of the design.

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High Speed Memory Layout Considerations

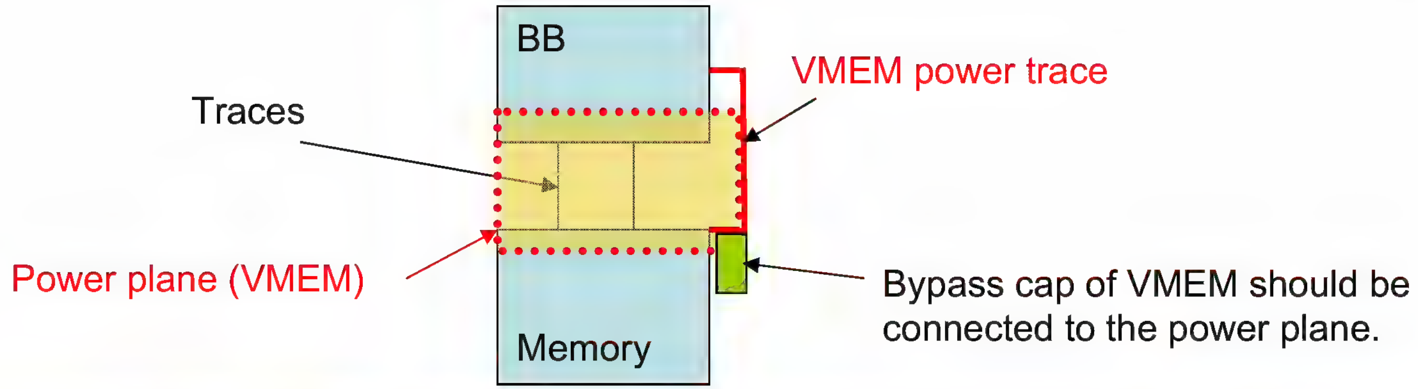
- Ground/Power plane
  - A solid power/ground plane must be provided near all traces routing layers.
  - It will minimize the ground return current to get better performance.
  - There are 2 methods for reference:
    1. It is recommended all traces are routed above a solid GND plane, and there is a power plane (memory power domain) under the GND plane if possible.

       e.g. 1st layer : Traces

       $2^{nd}/3^{rd}$ layer: Trace (strongly recommended - the same group of traces routed on the same layer)

       4rd layer: GND

       5th layer: Power plane (VMEM) if possible, which is under the traces of memory interface.



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High Speed Memory Layout Considerations

2. All traces are routed above a solid GND plane , and under a DC power plane (VBAT domain) to provide good shield (the traces of memory interface protected by VBAT and GND)

   e.g. 1st layer : VBAT

   2nd layer: Trace (strongly recommended - the same group of traces routed on the same layer)

   3rd layer: Trace

   4th layer: GND

Note: All power trace bypass capacitors must be placed as close to the devices' power pins as possible, and all capacitor's GND should have the shortest and widest trace to the GND plane.

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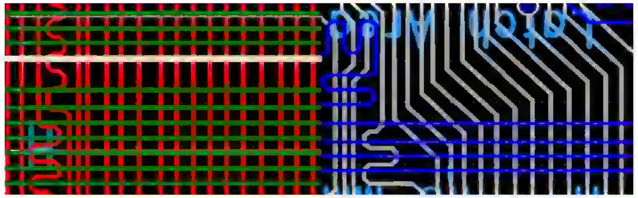
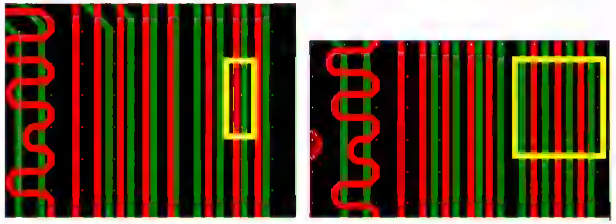
Suggested Layer Definition

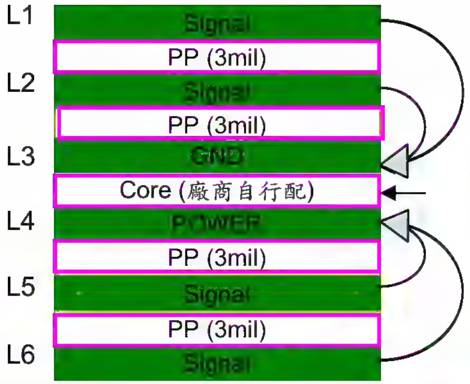
- Layer definition
  - 相鄰層避免走平行線

6 Layer for EVB	
L1	Signal (vertical)
L2	Signal (horizontal)
L3	GND
L4	Power
L5	Signal (vertical)
L6	Signal (horizontal)


(0)


(X)

- Stack-up



PP厚度較薄,L1及L2的Signal有最短的 return path

建議CORE的厚度最厚,以保持其它層的PP厚度較薄

PP厚度較薄,L5及L6的Signal有最短的 return path

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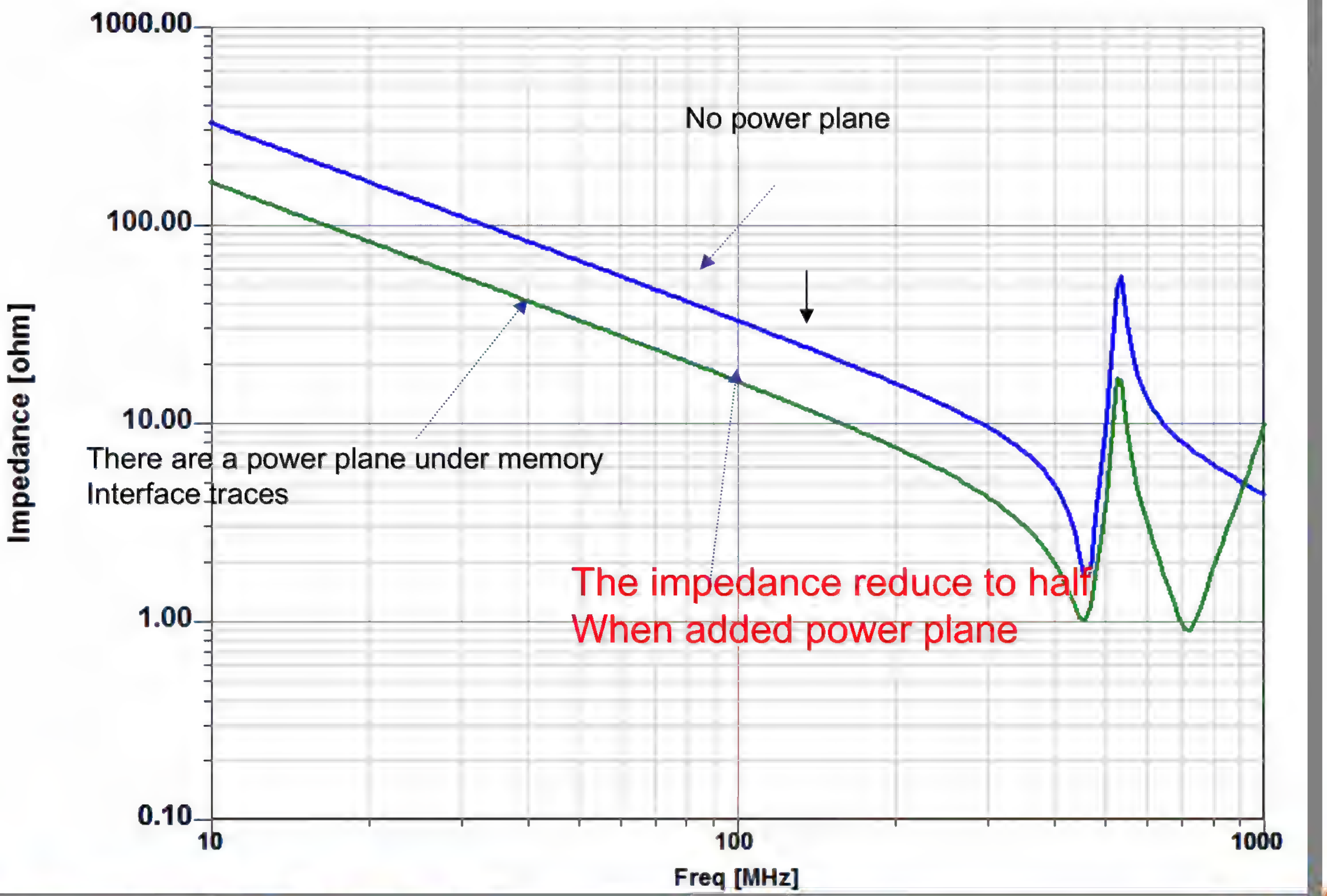
High Speed Memory Layout Considerations

- If we take a good power plane under traces, we can get good power trace impedance performance.



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High Speed Memory Layout Considerations

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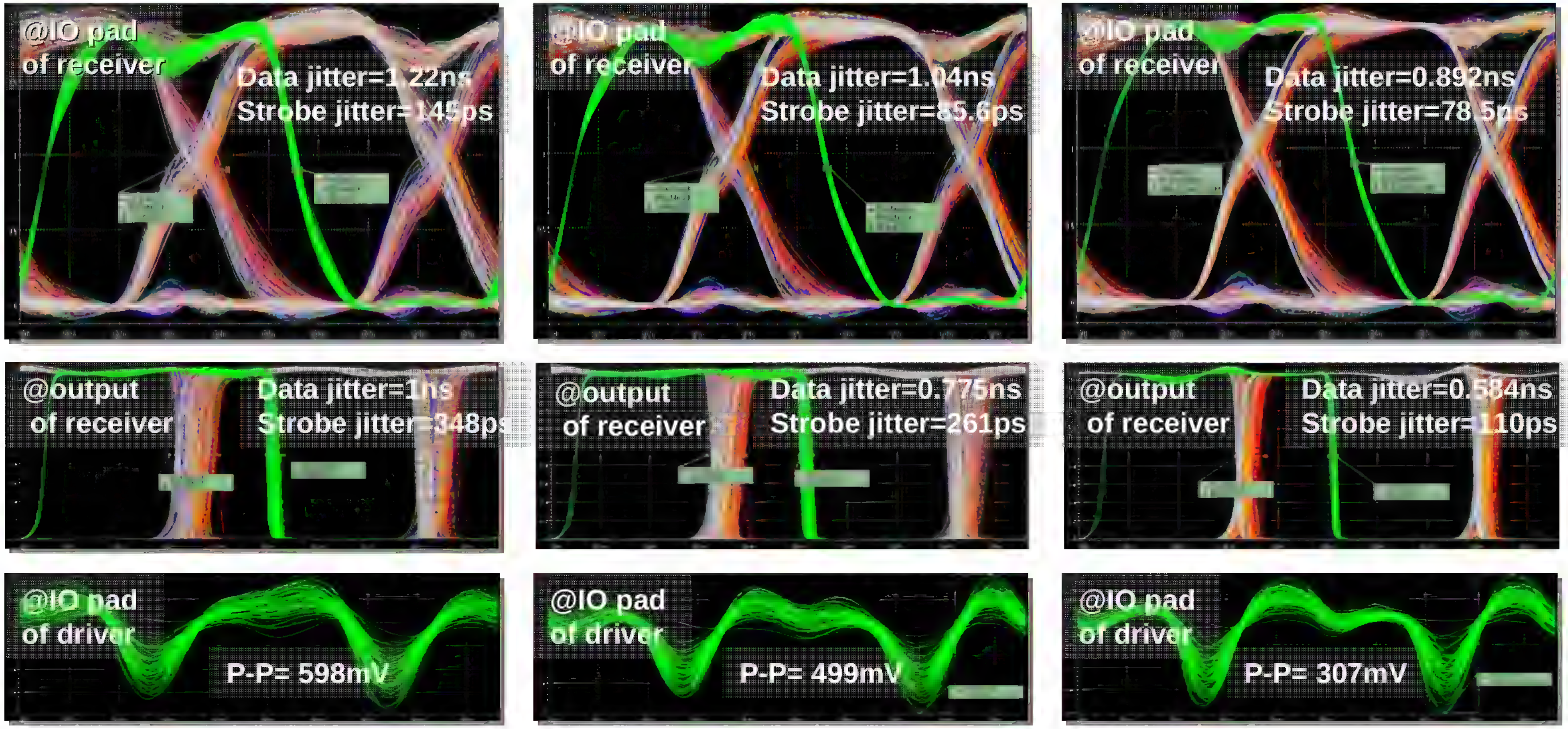
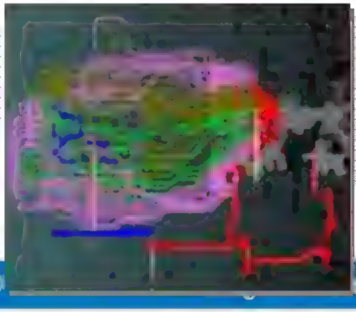
Add a power plane on PCB to enhance performance (reducing signal jitter)



Only power trace
Not good



Added a small power plane under BB chip
Better

Added power plane under BB chip and DRAM
Best

High Speed Memory Layout Considerations

Signal layout

- We categorized all signals into 4 groups, prioritized as follows:
  - 1st priority: Data group
  - 2nd priority: Clock group
  - 3rd priority: Control/Command groups
- If possible, control trace impedance between BB chip and DRAM, trace impedance is related to PCB dielectric constant, trace width, trace thickness, and routing method (using microstrip or stripline).
- The performance will get better if signal trace impedance is under control.

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask
Clock	CLK CLK#	Memory Differential Clock Memory-inverted Differential Clock
Command	A[0:15] BA[0:1] RAS CAS WE	Address Bus Bank select Row Address Select Column Address Select Write Enable
Control	CKE CS	Clock Enable Chip Select

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High Speed Memory Layout Considerations

1. Data group (1/2)
   – DQx and DQS must be routed in a group and routed in the same layer and reduce via counts if possible.
     e.g.
     D[0:7] is aligned to DQS[0];
     D[8:15] is aligned to DQS[1].
     So, D[0:7] must be routed in a group with DQS[0],
     and D[8:15] must be routed in a group with DQS[1].

Group	Signal Name	Description
Data	DQ[0:15] DQS[0:1] DM[0:1]	Data Bus Data Strobe Data Mask

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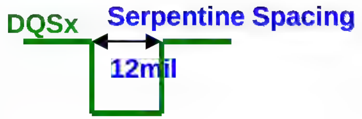
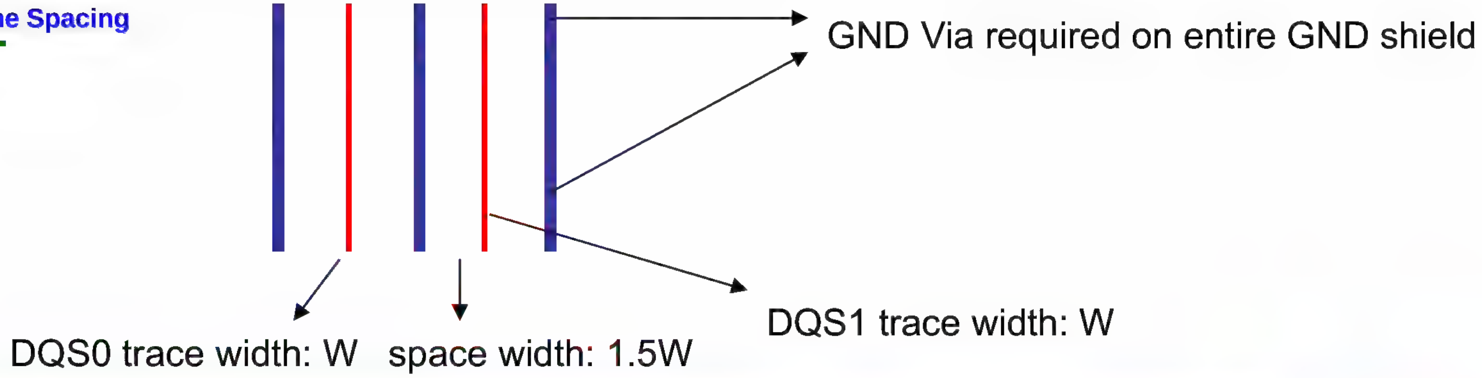
High Speed Memory Layout Considerations

1. Data group (2/2) (Remind : power/GND plane is the most important)
   - Within the same data group: (Max. trace length – 500 mil)< Trace length < (Max. trace length)
   - Between different data group: (Max. trace length – 500 mil)< Trace length < (Max. trace length)

     | DQS - Clock trace length | < 300 mil
   - If possible, control data trace impedance to ensure it meets the requirement (please check input impedance of memory).
   - Within the same group if DQx trace width is W, the space between DQx is 1.5 W.
   - To reduce the crosstalk on DQSx , GND shielding is required.
   - If the trace width is W , the trace space between DQSx and GND is at least 1.5W, and the width between DQS0 and DQS1 is at least 3W.
   - Do not route data group traces in parallel for a long distance.





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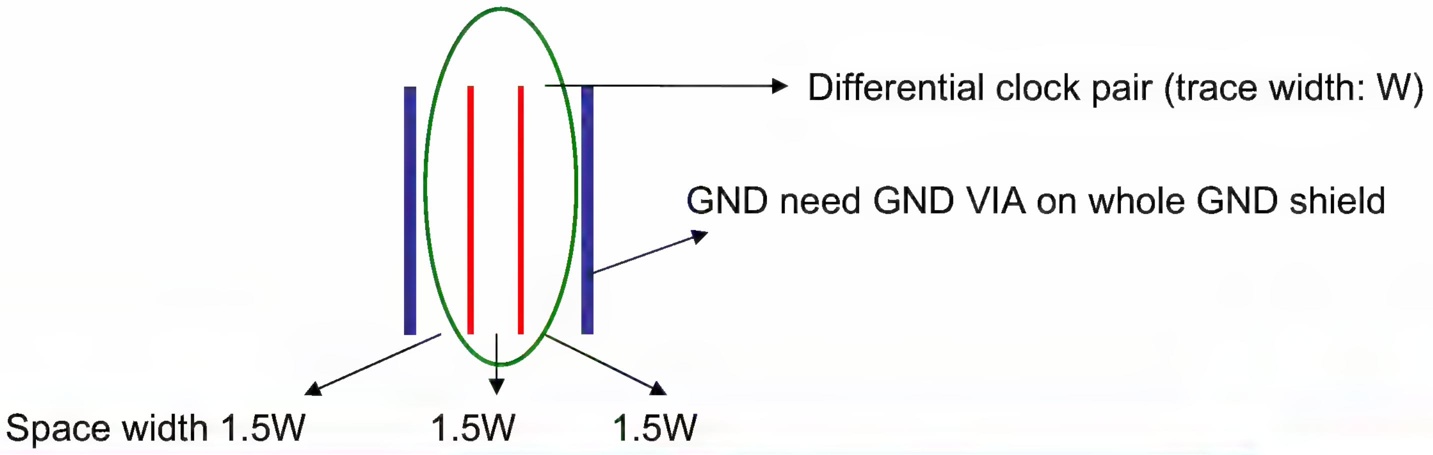
High Speed Memory Layout Considerations

2. Clock group (1/2)

- There are a differential pair of high speed clocks in the DDR SDRAM memory device, so we need to take care of these traces to ensure the clock integrity.
- Route these 2 clock traces in parallel and keep equal trace length.
- Control clock trace impedance (please check memory device). If clock trace is W the space between clk and /clk is at least 1.5W and there need GND shield wrap around the clock differential pair. The space GND and Clock trace at least 1.5W , and the GND shield need enough GND via if we can not give enough GND via , we would rather take GND shield off , and the space to adjacent signals is at least 2W.



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High Speed Memory Layout Considerations

2. Clock group (2/2)

- Away from other high frequency traces
- Each clock trace must have solid power and ground plane near the entire route.
- Each clock trace is recommended to route on the same layer to reduce Via number, and to keep the same trace characteristics.

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High Speed Memory Layout Considerations

3. Control/Command groups

- Every trace must have solid power and ground plane near the entire route.
- Every trace is recommended to route on same layer to reduce Via number, and to keep the same trace characteristics.
- Route address traces from priority A0 (most toggled) to A15 (less toggled), and A0 should be close to ground if possible.
  |Trace length - Clock trace length| < 500 mil

  Within CMD/ADR group:
  |Max. (CMD/ADR trace length) – Min. (CMD/ADR trace length)| <250 mil
- Remind : power ground is the most important , you just need to meet the traces match criterion as possible
- If serpentine is needed , the spacing is at least 12mil

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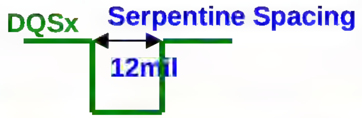
Check List

- Placement
  - Memory device must placed as close to the BB chip as possible.
  - Avoid extra long trace (Max. trace: 1500 mil) and other high frequency devices placed close to memory
  - Route these traces smoothly, reduce the Via counts and avoiding traces interlacing if possible
- Considerations on ground/power plane **(power/GND plane is the most important)**
  - It is recommended all traces to be routed above a solid GND plane, and there is a power plane (memory power domain) under GND plane if possible.

    e.g. 1st layer: Traces
    2nd layer: Trace (strongly recommended — the same group of traces routed on the same layer)
    3rd layer: GND
    4th layer: Power plane (VMEM) if possible, the plane is under the traces of memory interface.
  - Or all traces are routed above a solid GND plane, and under a DC power plane (VBAT domain) to provide a good shield (the traces of memory interface protected by VBAT and GND).

    e.g. 1st layer : VBAT
    2nd layer: Trace (strongly recommended — the same group of traces routed on the same layer)
    3rd layer: Trace
    4th layer: GND
- Trace length is as match as possible , All traces refer to clock , within 500mil length difference is acceptable (DDR , DQS and DQ is a group , and DDR clock ,/clock are within 100mil)
- If serpentine is needed , the spacing is at least 12mil



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MT6516 USB Design Notes

Schematics and Cable Design

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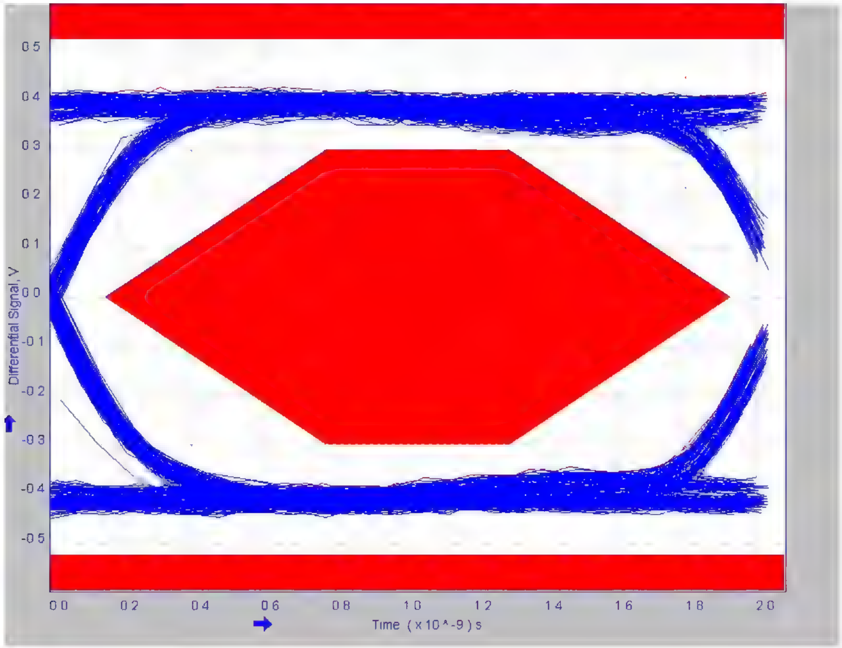
MTK USB2.0 Solution Introduction

- This document introduces MTK USB2.0 design and some points for attention.
  - MTK USB2.0/ OTG device can operate at USB2.0 High-Speed (HS) mode (480Mb/s) and Full-Speed (FS) mode (12Mb/s).
- General HS eye diagram is shown as below. The output swing is differential 0.4V. Bad eye diagram will lead to certification fail or signal integrity problem.



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USB Pin Definition

- USB2.0 pin out description.
  - General pins

Pin	Symbol	Type	Description
1	PAD_USB_VBUS	IO	* Comparator used for detecting changes of VBUS voltage.
2	PAD_USB_DM	IO	USB serial differential bus (minus)
3	PAD_USB_DP	IO	USB serial differential bus (positive)
4	AVDD3_USB	VDD	Analog 3.3V supply
5	AVSS33_USB	GND	Analog 3.3V ground
6	PAD_USB_VRT	IO	Analog 5.1K reference resistor
7	AVDD12_USB	VDD	Analog 1.2V supply.
8	AVSS12_USB	GND	Analog 1.2V ground

  - Optional pins for supporting OTG

Pin	Symbol	Type	Description
9	PAD_USB_ID	IO	Optional function for USB OTG ID pin for detecting slave plug in.

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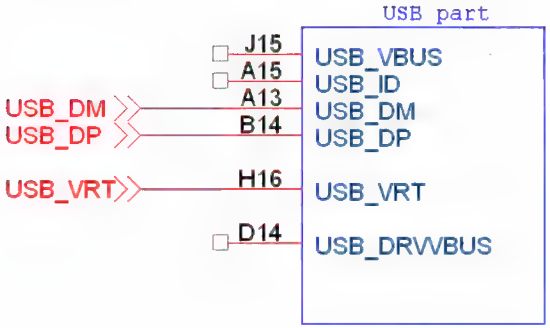
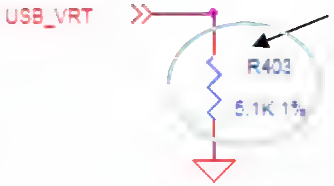
Schematics Design for USB2.0 Device (2/2)

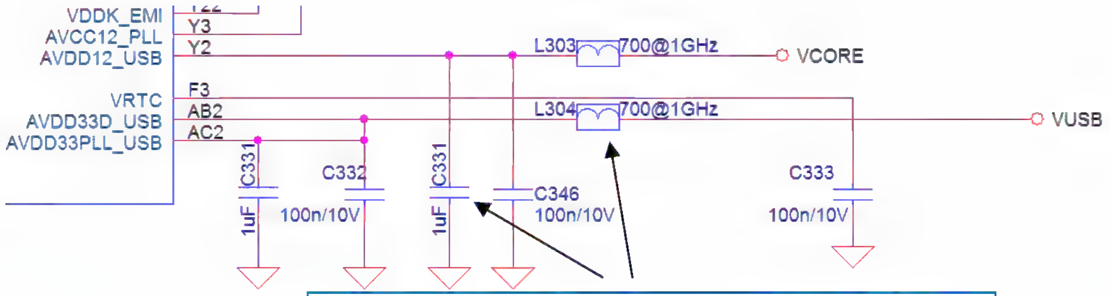
- MT6516 (Device Only)



Don’t have to connect VBUS/ID



Must be 5.1K ohm, 1%
Place close to IC



Reserve bead and bypass capacitor for USB 1.2, 3.3V Power

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Schematics Design for USB2.0 High Speed

- Beware of USB_VRT pin should keep away from noise source and high speed clock data like camera databus.
- Reserve 0402 cap (NC) on DP/DM for ESD protection and rise time/fall time tuning for USB-IF compliance test.
- If want to get USB-IF OTG logo, should use micro-AB connector.

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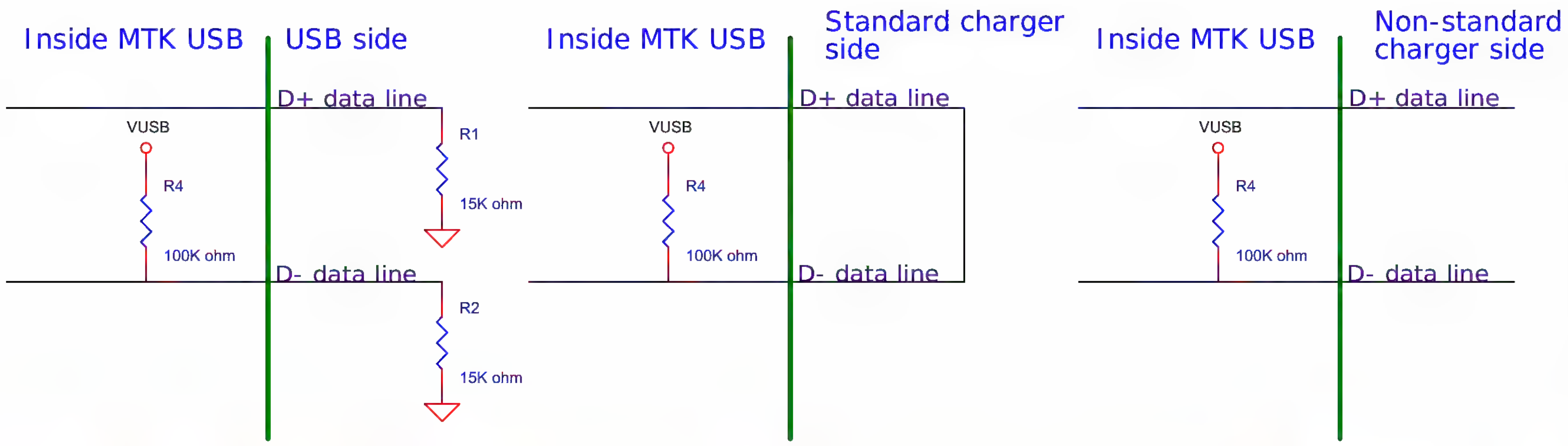
USB/ Charger Detection

- Used for MT6516 and later on MTK ICs (MT6268/MT6516/MT6253)
- When charger interrupt happens, turn on D- pull high 100K ohm resistor and check the polarity of D-
  - If the D- is LOW, it is USB charger, otherwise it is a standard or a non-standard charger



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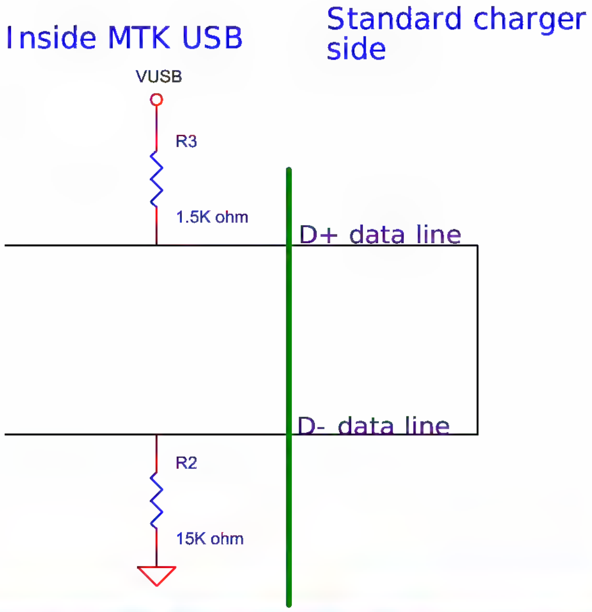
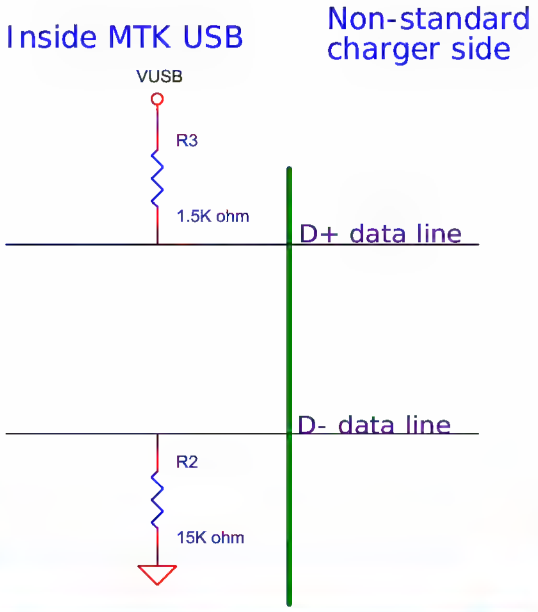
USB/ Charger Detection (Cont.)

- Then check whether it is standard or non-standard charger. Turn on D+/D- internally 15K ohm pull low resistor and D+ 1.5K ohm pull high resistor at the same time.
  - Check D- polarity. If the D- is HIGH, it is standard charger, otherwise it is a non-standard charger.





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High Speed USB Layout Checklist (1/2)

- General design and layout rules
  - With minimum trace lengths, route clock source and HS USB differential pairs first. Keep maximum possible distance between clocks/periodic signals to USB differential pairs to minimize crosstalk.
  - Route HS USB signal pairs together with equal length by using a minimum vias and corners. This reduces signal reflections and impedance changes.
  - Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance.
  - When it becomes necessary to turn 90° , use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
  - Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.

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High Speed USB Layout Checklist (2/2)

- General design and layout rules (Conti.)
  - Stubs on HS USB signals should be avoided, as stubs will cause signal reflections and affect signal quality.
  - Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical.
  - Keep HS USB signals away from high current area. The current transient during state transitions could induce noise to USB.

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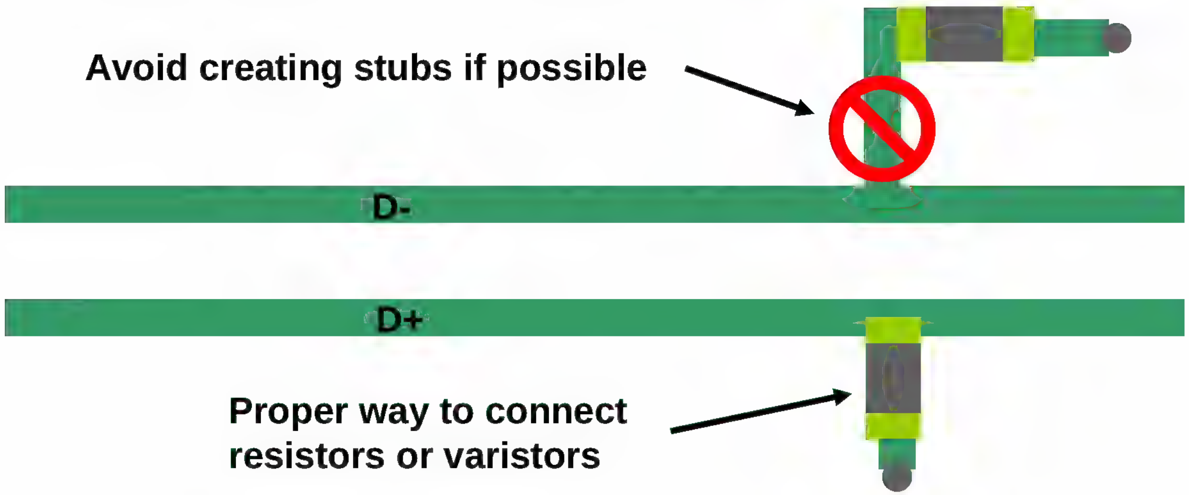
Stubs

- Avoid creating unnecessary stubs on data lines, if a stub is unavoidable (for example: ESD issue), please keep the stub as short as possible.



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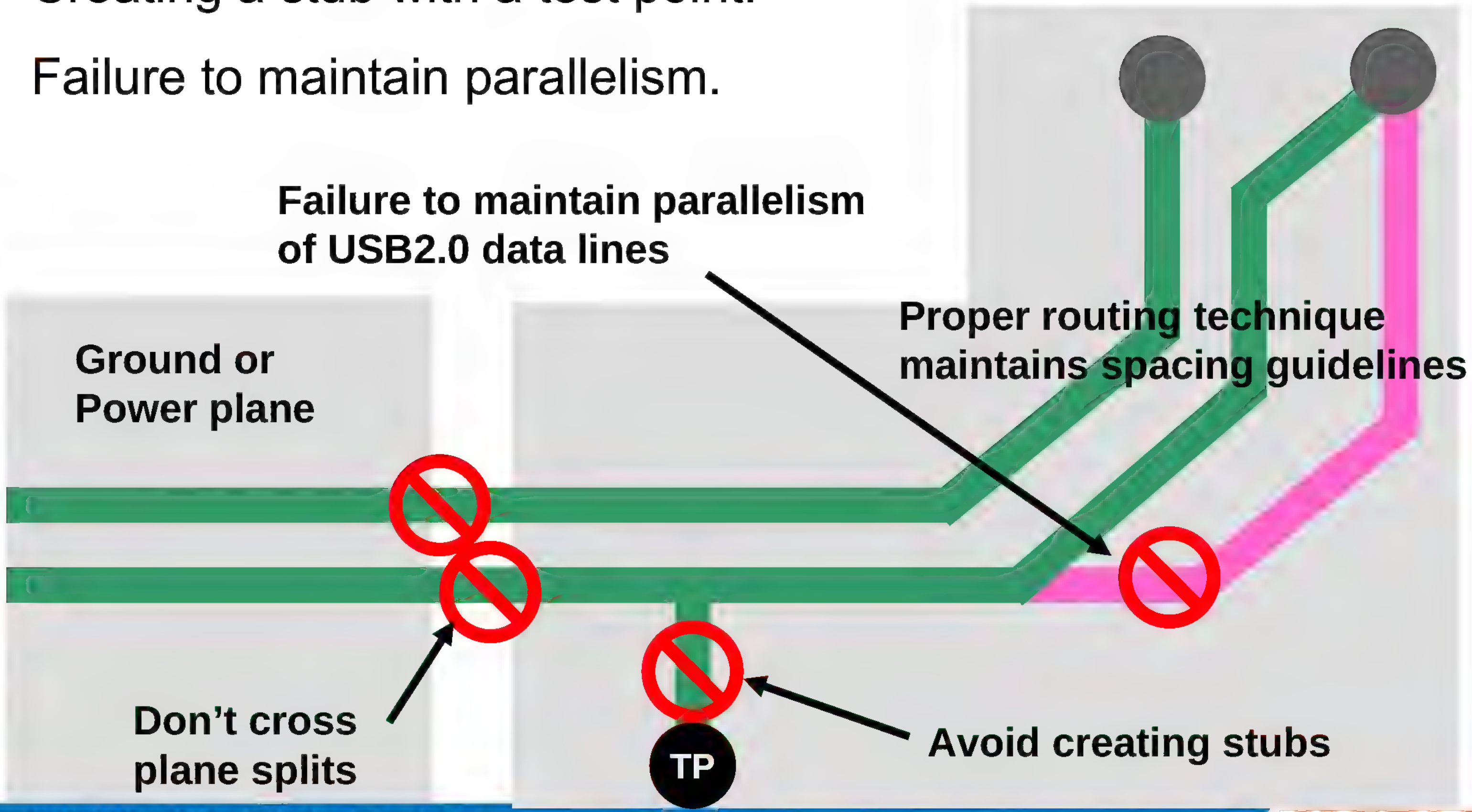
Poor Routing Techniques

- Cross a plane split.
- Creating a stub with a test point.
- Failure to maintain parallelism.



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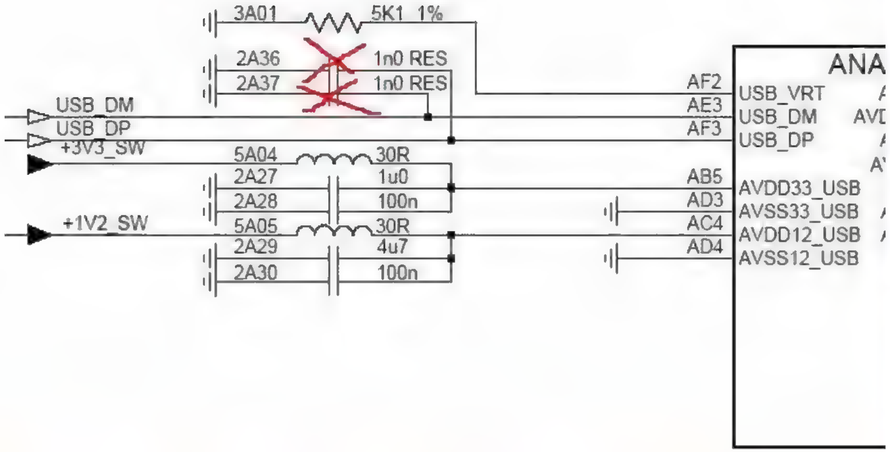
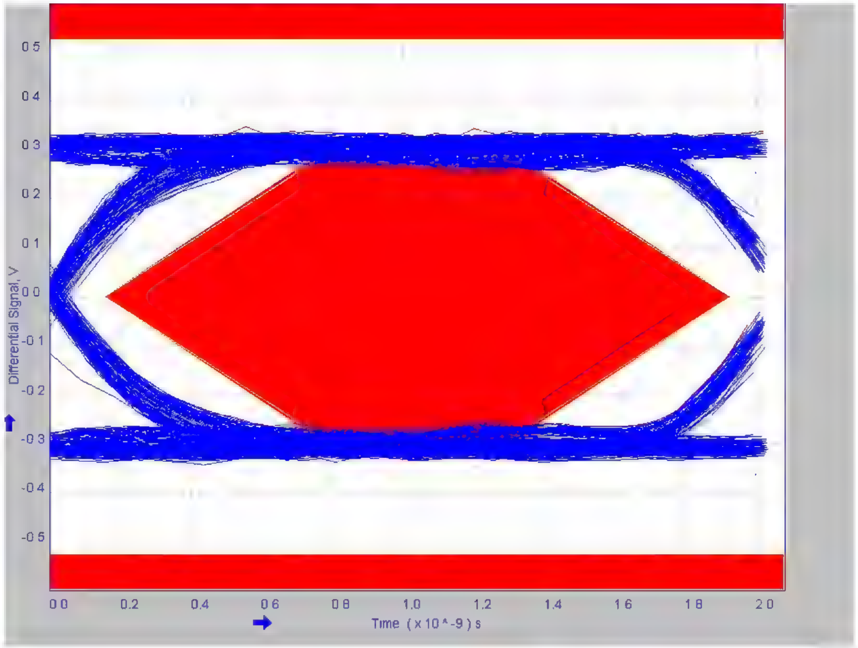
Case Study (1/5)

- Case 1:
  - 2A36/2A37 should be removed. Large cap at USB_DP/USB_DM will lead to bad jitter performance.
  - Measured eye at board is shown below. It will occur turn-around error at system application.





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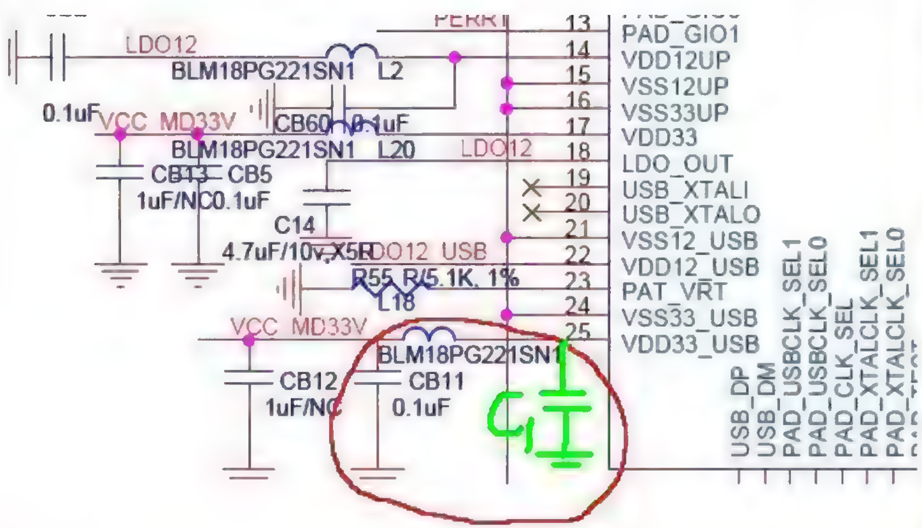
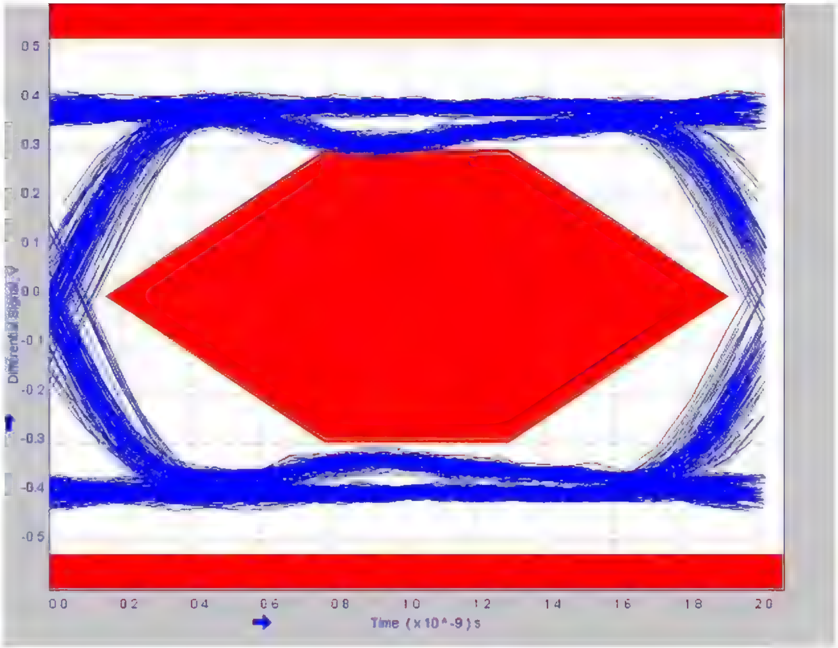
Case Study (2/5)

- Case 2:
  - After bead, at least 0.1uF capacitor between VDD33_USB, VDD12_USB and ground must be added as follows.
  - Measured eye diagram has bad jitter performance.





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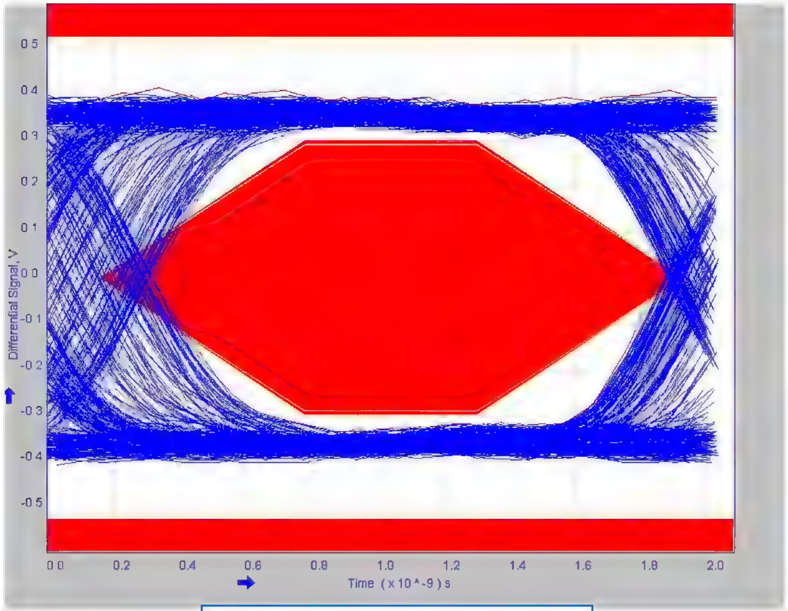
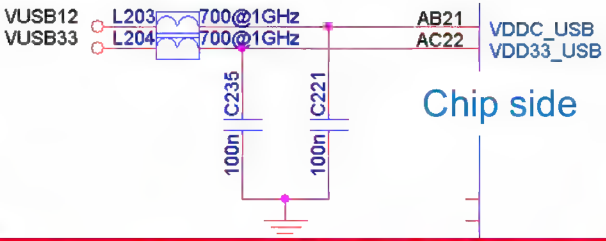
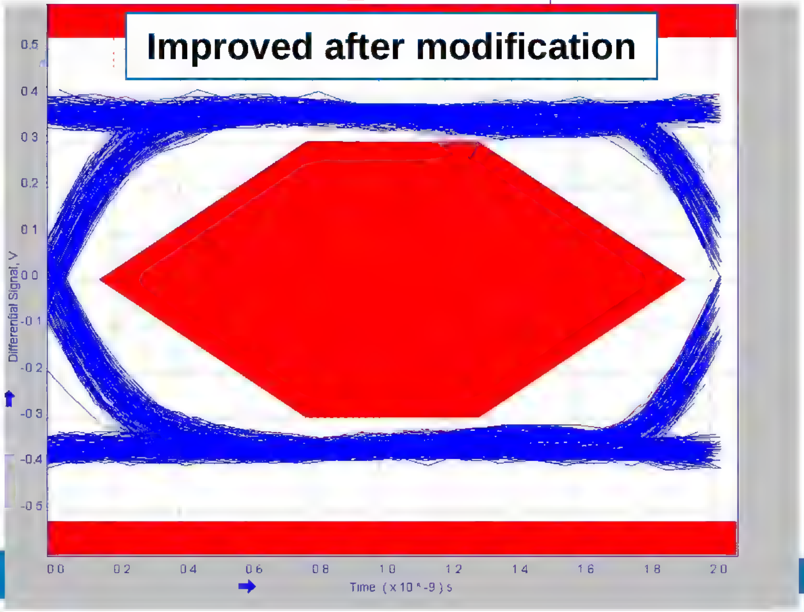
Case Study (3/5)

- Case 3:
  - Some time we got worse jitter due to poor layout, then VUSB33 and VUSB12 are coupled by noise.
  - It is improved by increasing bypass capacitor C221 and C235.



Before modification





Improved after modification

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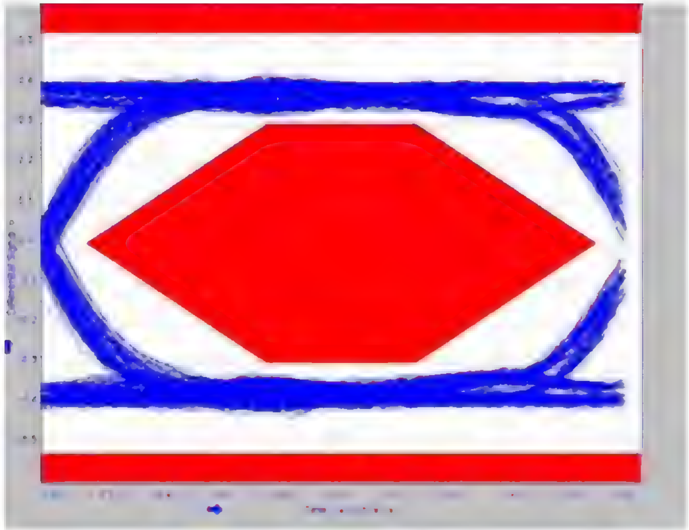
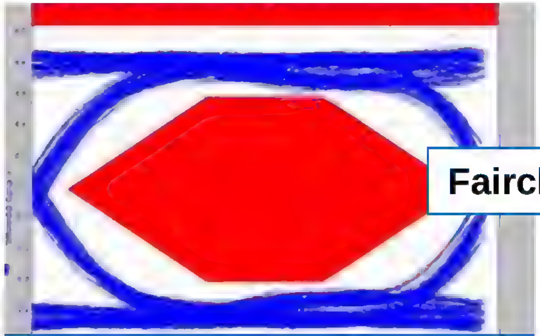
Case Study (4/5)

- Case 4:
  - Customer wants to share USB data pins with audio/UART pins through the same 5-wire USB connector by using analog switch.
  - Different analog switches cause different attenuation of signals; please make sure component and layout will get proper eye diagram.
  - No suggestion on using analog switch, 11-pin USB connector could be used instead.

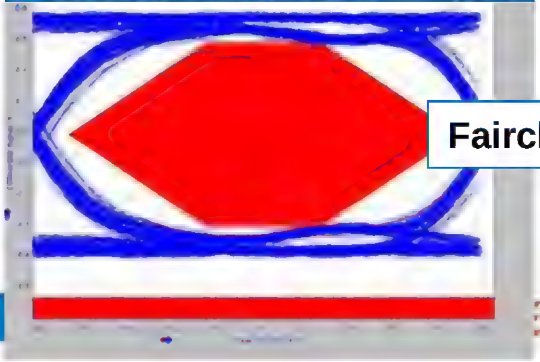


Original design without analog switch

Add different analog switch



Fairchild FSUSB42



Fairchild FSUSB30

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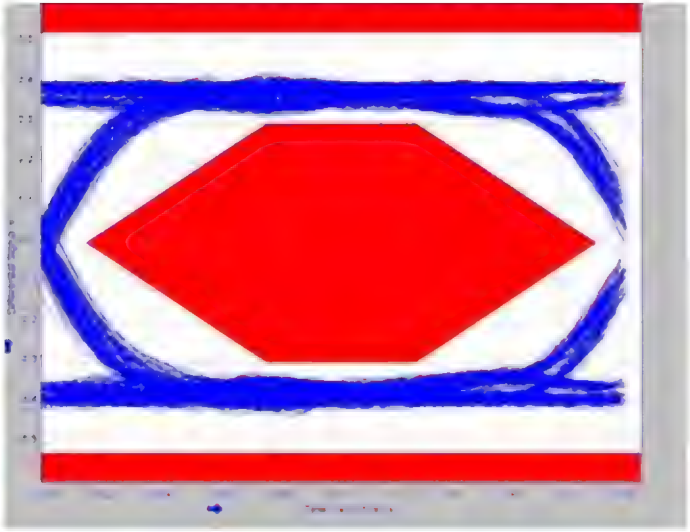
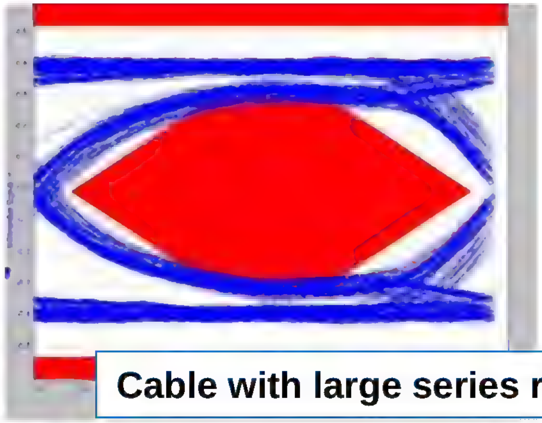
Case Study (5/5)

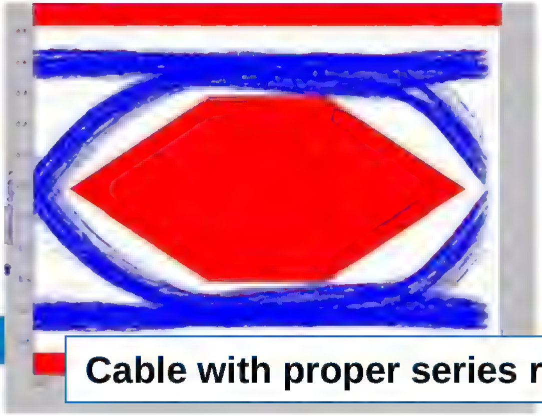
- Case 5:
  - Sometimes customer may design a special connector for USB, such as 18-pin I/O.
  - Poor cable will cause poor performance.
  - Please follow USB cable design guide.



Design with normal USB cable



Cable with large series resistance



Cable with proper series resistance

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Conclusions

- Layout and component selection are critical for USB2.0 high speed performance
  - Need to follow the design rule or there might be compatibility issue happens
- Grounding and shielding are both critical when design USB2.0 high speed capable cables
  - It can maintain USB signal quality with little jitter/ signal distortion caused by cable design
- Please refer to "MTK USB2.0/ OTG Design Guide " for more detail.

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MT6516 Factory Mode & Engineer Mode Notice

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Engineer Mode and Factory mode

- Factory mode
  - Enter phone menu
  - Enter "*#66*# ", then dial
- Engineer mode
  - Enter phone menu
  - Enter "*#3646633#", then dial

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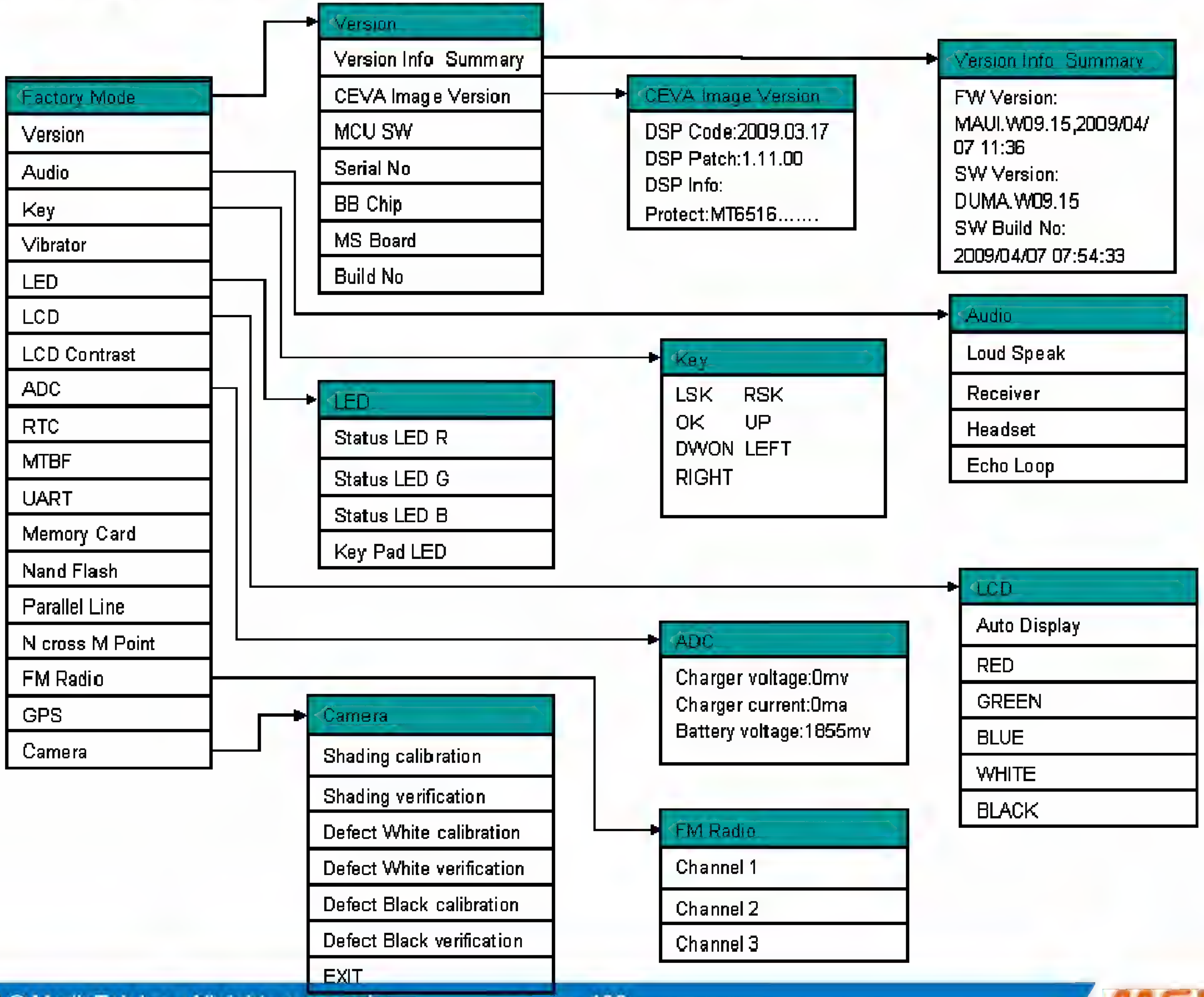
Factory Mode Menu Tree



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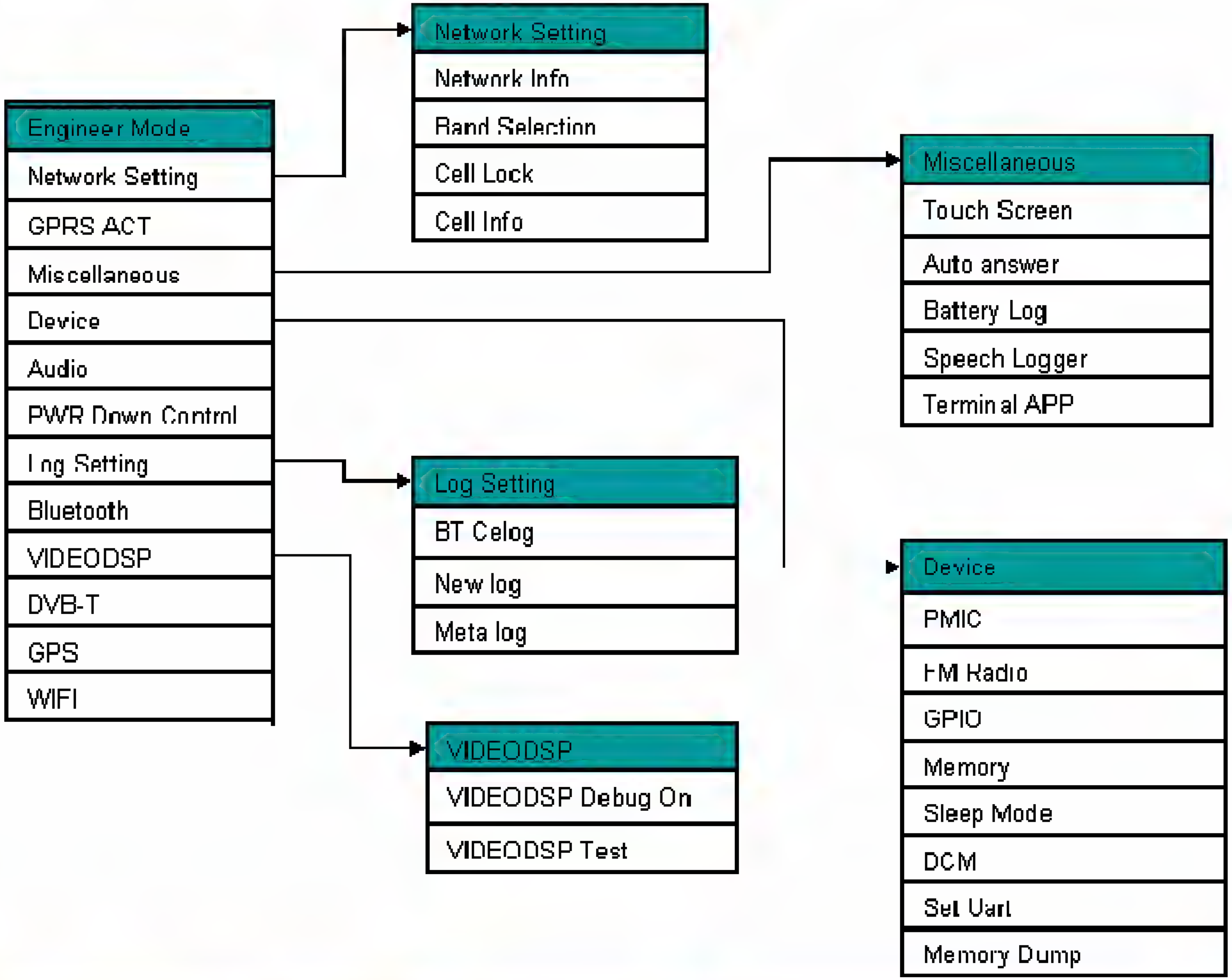
Engineer Mode Menu Tree



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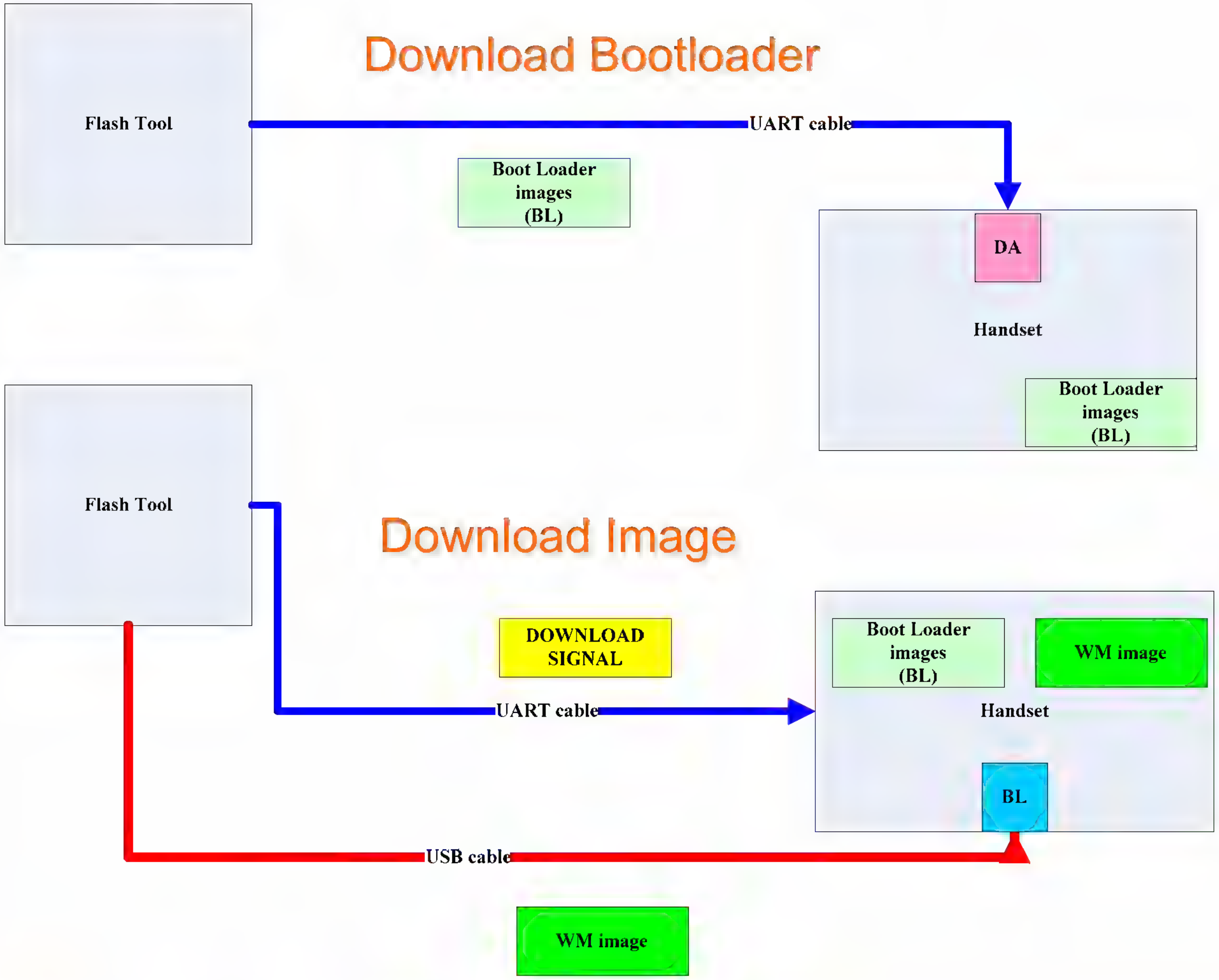
Flash Tool Download Flow



- Bootloader Download
  - Use UART1 to download bootloader
- Windows Mobile image download
  - Connect both UART1 and USB to download full WinMo image
- Flash tool can combine the two steps above. (Must connect both UART1 and USB to PC first !)
- Please refer to flash tool document in detail.

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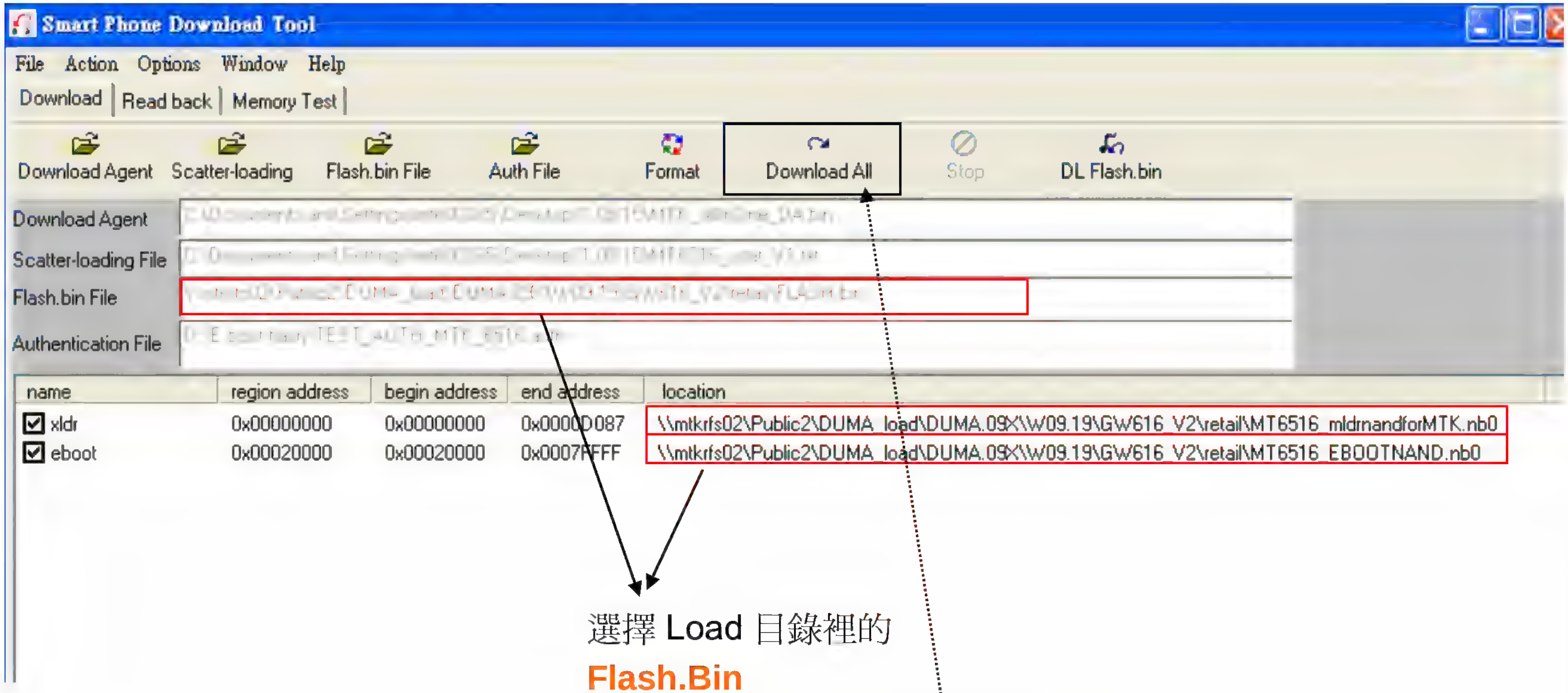
Download tool



選擇 Load 目錄裡的

Flash.Bin

MT6516_mldrnandforMTK.nb0

MT6516_EBOOTNAND.nb0

Then press Download all

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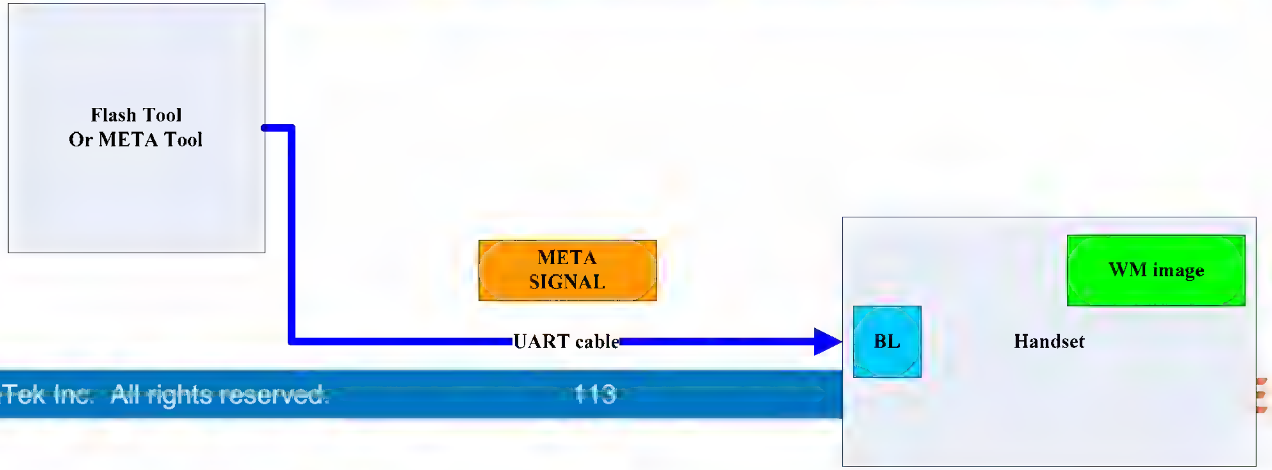
META Link (AP Side)

- Install Smartphone META tool.
- How to enter META mode (UART1)
  - If target have not been in META mode, click "Reconnect" button, then connect phone;
  - Phone will power on and enter into META mode automatically
- UART can support up to 115200bps baud rate



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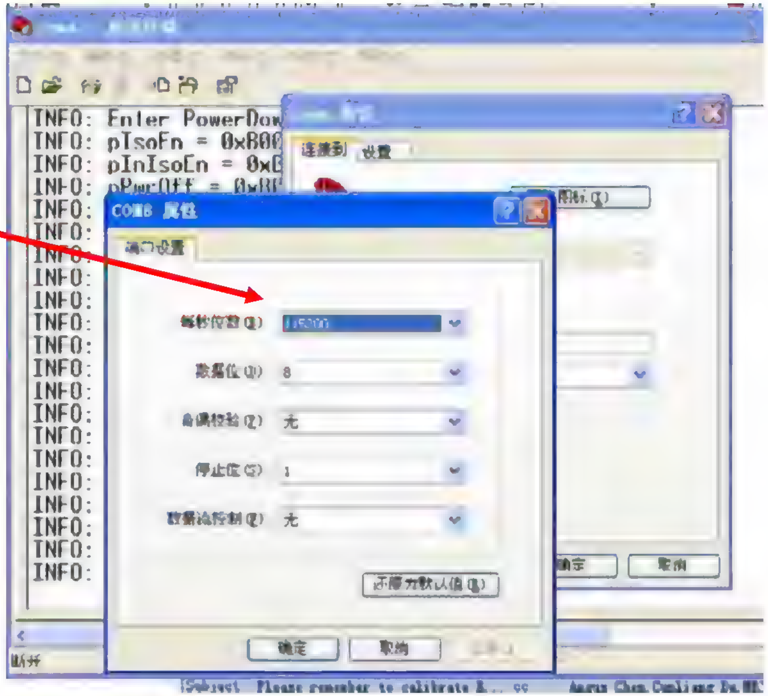
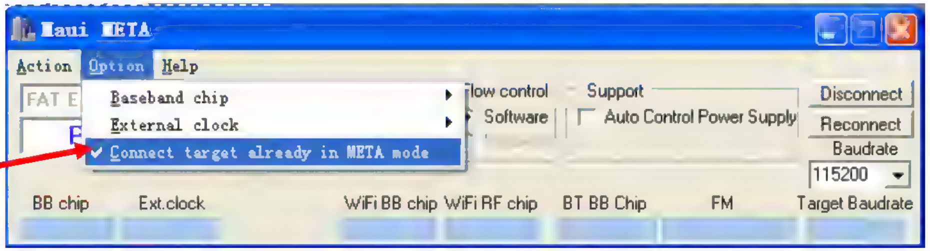
META Link (Modem Side)

- Install smartphone META tool (for first time)
- Link UART4 on handset to PC
- Open hyper terminal on PC and set correct COM port and parameters.
- Press “send key” and “end key” to power on.

```
INFO:SPAR2: [fdce]...
INFO: enable wake_up pmic...
INFO: g_bootContext.rebootFlag = 0
                INFO: OEMPreDownload: CONFIG..
                INFO:BootLoadNandCfg: Found Cc
Hit space to enter configuration menu 5...
Hit space to enter configuration menu 4...
Hit space to enter configuration menu 3...
```



- Set boot to META mode: Enter 9->3->1
- Enter 0->0, continue to boot to META mode
- Close hyper terminal, switch UART4 to UART1. (UART1 link to PC)
- Wait about 12 seconds.
- Execute META tool
- Choose UART and enable “connect target already in META mode” in option menu.



- Can backup/restore calibration data in “update parameter” as feature phone.

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MT6516 Memory Support Plan

MTK MVG (Memory Verification Group)

Apr 2009

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EDGE Smart Phone

Segment	EDGE Smart Phone
Platform	MT6516
MCP	(2G/1G) +1G (x32) NAND + MobileDDR MCP
MCP Type	NAND(SLC, 2K page) + 133/166MHz MobileDDR
Memory P/N (Week available)	Samsung K522F1GACM-A060 (2G+1G, 1.8V*, BGA137) → W0919 Elpida EHD013011MA-60 (2G+1G, 1.8V, BGA137) → W0921 Toshiba TYA000B801CFLP40 (2G+1G, 1.8V, BGA137) → W0922 Numonyx NANDBAR4N5BZBC5E (2G+1G, 1.8V, BGA137) → W0923 Micron MT29C2G24MAKLAJA-6 (2G+1G, 1.8V, BGA137) → W0924 Hynix H8BCS0PJ0MCP-56M (1G+1G, 1.8V, BGA137) → W0925 Samsung K522H1GACD-A060 (2G+1G, 1.8V, BGA137) → W0926 Micron MT29C1G24MAVLAJA-6 (1G+1G, 1.8V, BGA137) → W0927 Micron MT29C1G24MACLAJA-6 (2G+1G, 1.8V, BGA137) → W0928

* Voltage supply of NAND flash.
** For devices not included in the weeks available, please contact with MTK PM for status update.

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Appendix

Peripherals Design Notice (GPS/DTV)

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MT6516
WIFI/BT Co-module Application Note

2009/4

WCP/RP1/W.Wei

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Outline

- **Module function block and reference design**
  - Module function block
  - Module reference design
  - Reference interface assignment
  - Key component list

- **Schematic and layout design guide**
  - Schematic design guide
  - Layout design guide

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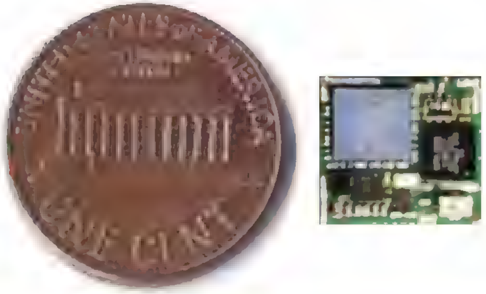
Wi-Fi/BT Combo Module Product Definition

- Full-featured Wi-Fi 802.11b/g and BT 2.1 + EDR combo module
- Small-size package: 9.5×10.5×1.4 mm LGA (< 10×10 mm)
- MTK's proprietary superior Wi-Fi/BT co-existence performance
- Wi-Fi and BT co-existence shares the 26 MHz clock frequency.
- Metal EM interference shielding
- Antenna: Dual antenna (mandatory)/Single antenna (optional)
- RoHS complaint



Sample: Sep. 2008

MP: 2009/02

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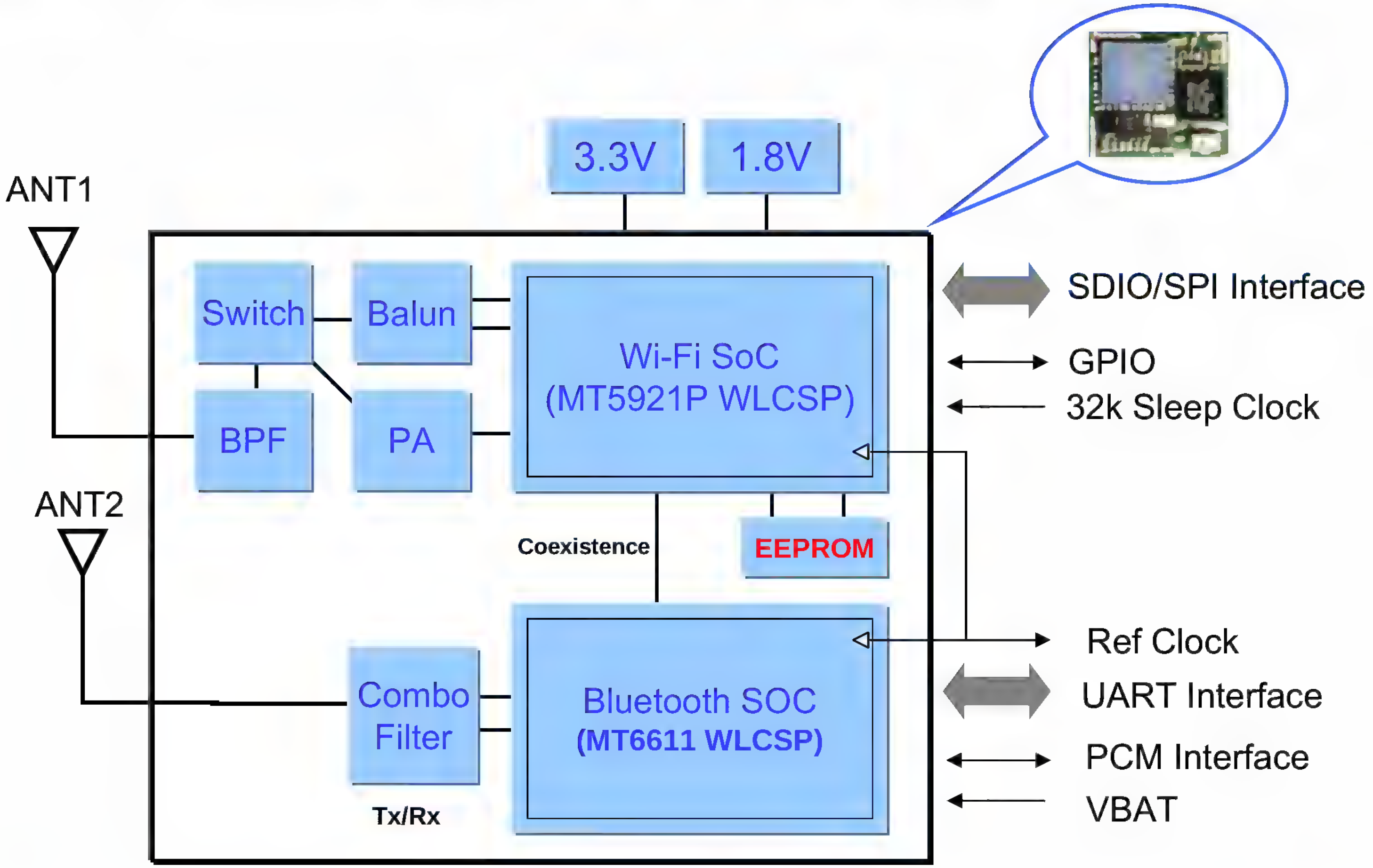
MTK Combo Module Block Diagram



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Wi-Fi Features

- Advanced Wi-Fi features
  - 802.11b/g/e/i/h/k/w compatible
  - IEEE 802.11e QoS (WMM/WMM-PS)
  - Background scan for specific SSID networks
  - IEEE 802.11i advanced security (WEP/TKIP/AES/WPA/WPA2)
  - 802.11e optional U-APSD, DLS
  - 802.11 power saving mode
  - Wakeup by specific packet (pattern search)
  - Thermo-sensor to resist temperature change
- Voice over WLAN (VoWLAN)
  - UMA (Unlicensed Mobile Access) technology
  - VoIP over WLAN
- Software support
  - Win CE 5.0
  - Win Mobile v5.0/6.1
  - Win Mobile v7.0 (planning)
  - Linux v2.6 (planning)
- Wi-Fi certified

http://certifications.wi-fi.org - Certification Standards - Microsoft Internet Explorer

Wi-Fi® Interoperability Certificate — Certification ID: WFA4688

This certificate indicates the capabilities and features that successfully completed interoperability testing by the Wi-Fi Alliance. You may find detailed descriptions of these features at www.wi-fi.org/certification_programs.php

Certificate Date: October 26, 2006
Category: Phone, dual-mode (Wi-Fi and cellular)
Company: MediaTek Incorporation
Product: Superman29 Dual Mode Phone
Model/SKU#: SUPERMAN29 DEMO

This product has passed Wi-Fi certification testing for the following standards:

IEEE Standard	Security	Multimedia
802.11b	WPA™ - Personal	WMM®
802.11g	WPA™ - Enterprise	WMM Power Save
	WPA2™ - Personal	
	WPA2™ - Enterprise	
	EAP Type(s)	
	EAP-TLS	
	EAP-TTLS/MSCHAPv2	
	PEAPv0/EAP-MSCHAPv2	
	PEAPv1/EAP-GTC	
	EAP-SIM	

For more information: www.wi-fi.org/certification_programs.php

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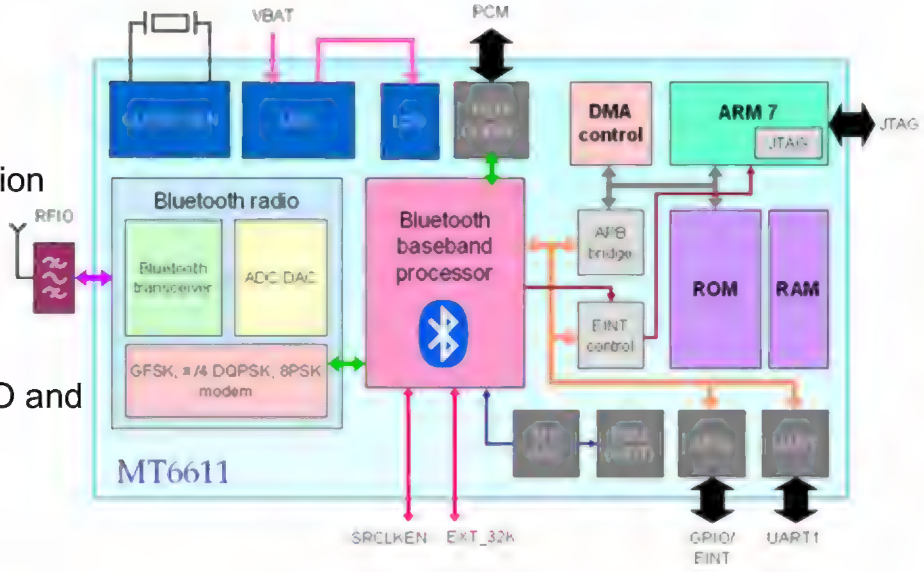
Bluetooth Features

- Radio features
  - Fully compliant with Bluetooth 2.1+EDR
  - Low-IF Architecture with high performance linearity
  - Supports Bluetooth class 2 and 3
  - Tx transmit power: 4 dBm
  - 90 dBm sensitivity with excellent interference rejection performance
  - 3.5 x 3.5 x 0.6 mm (max.), 0.5 mm pitch WLCSP
- Baseband features
  - Up to 7 simultaneous active ACL links
  - Supports 3 simultaneous SCO and eSCO links SCO and scatternet
  - Supports lower power mode (Sniff, Hold and Park mode)
  - Ultra low power consumption in sleep mode
  - Supports AFH and PTA for WLAN/BT coexistence
- Software features
  - Supports standard HCI interface
  - Supports more than 15 profiles in MediaTek platform



MT6611 Function Block

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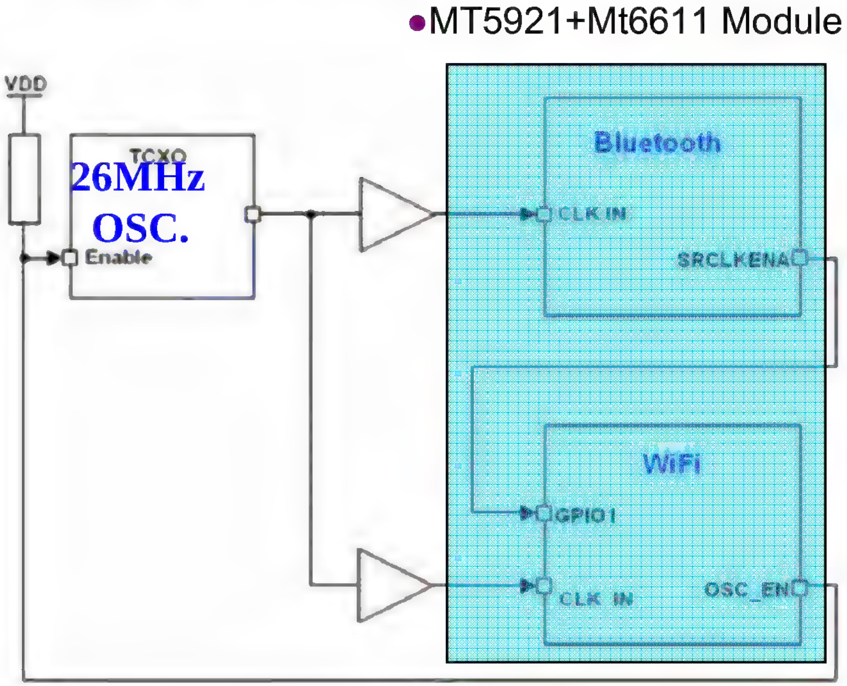
Module Share Clock with Daisy chain



- **WiFi power need to power on to keep daisy chain working normally.**
- **WiFi can be shut down only as BT power off.**

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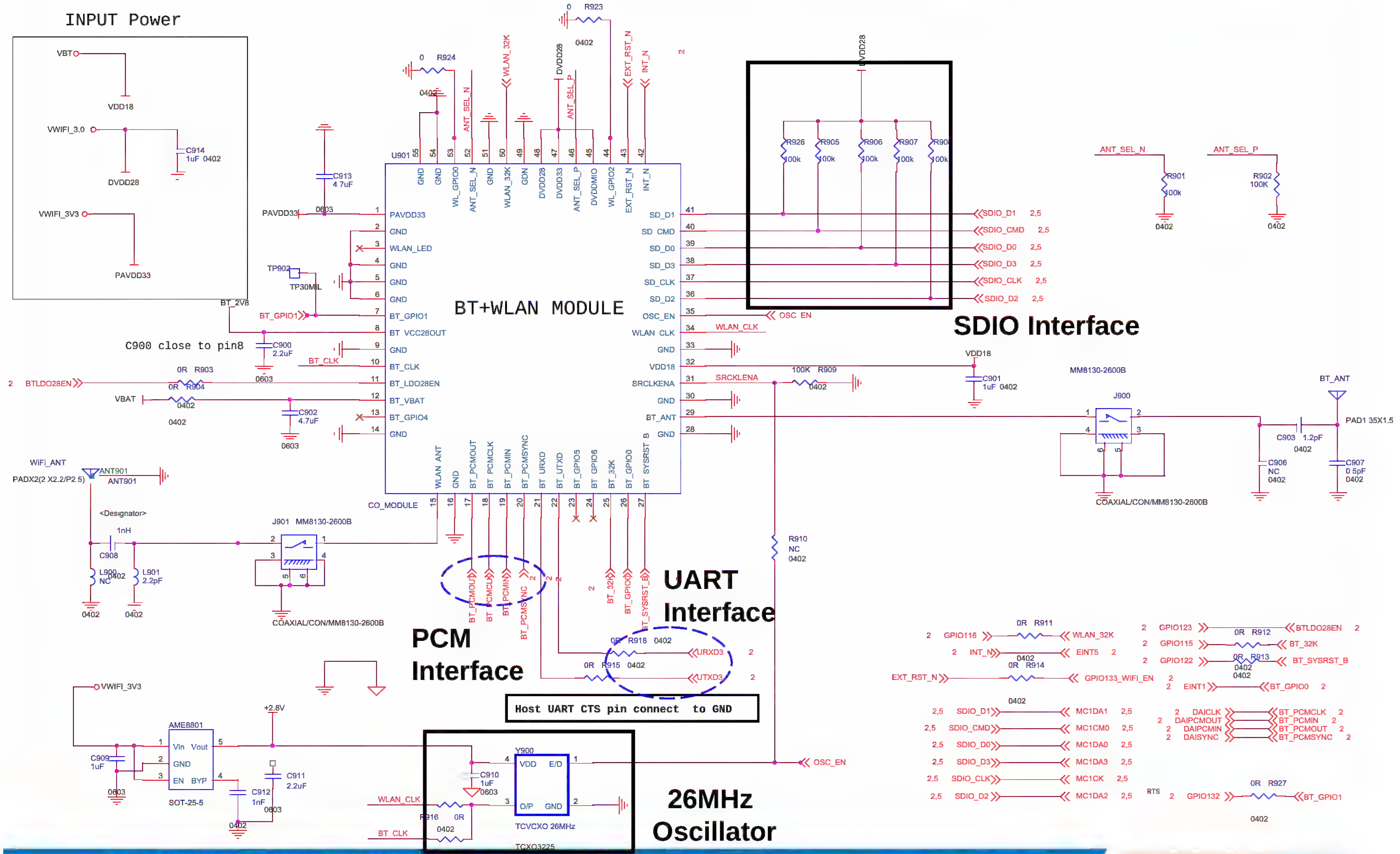
Co-module Reference Design



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Interface Assignment

Type	Pin	Function
I/O	GPIO133	WIFI_RSTB
	GPIO116	WLAN_32K
I/F	MC1CM0	SDIO
	MC1DA0	
	MC1DA1	
	MC1DA2	
	MC1DA3	
	MC1CK	
I/O	INT5	WiFi_interrupt

Type	Pin	Function
I/O	GPIO122	BT_RSTB
	GPIO115	BT_32K
I/F	UTXD3	UART
	URXD3	
	DAICLK	PCM
	DAIPCMOUT	
	DAIPCMIN	
	DAISYNC	
I/O	INT1	BT_interrupt

- MT6611 PCM/UART power domain support 2.8~3.3v, not support 1.8V

26MHz Oscillator List

Item	Part number	Vendor	Designator
26MHz Oscillator	SMA026000-3DR3T0 (Load 15pF, 2.8V~3.3V)	Aker	Y900
	8W26000011 (Load 15pF, 2.8V~3.3V)	TXC	Y900
	SG-310SCN. (Load 15pF, 2.8V~3.3V)	EPSON	Y900
	FK2600008 (Load 15pF, 2.8V~3.3V)	亞陶	Y900

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WiFi interface Selection

	TRSW_N	TRSW_N	ANT_SEL_P
SDIO	0	0	0
SPI	0	0	1

Main Clock Frequency Selection

	WLAN_ACT	ANT_SEL_P	OSC_FREQ0
20MHz	0	0	0
26MHz	0	0	1
40MHz	0	1	0

- Fixed

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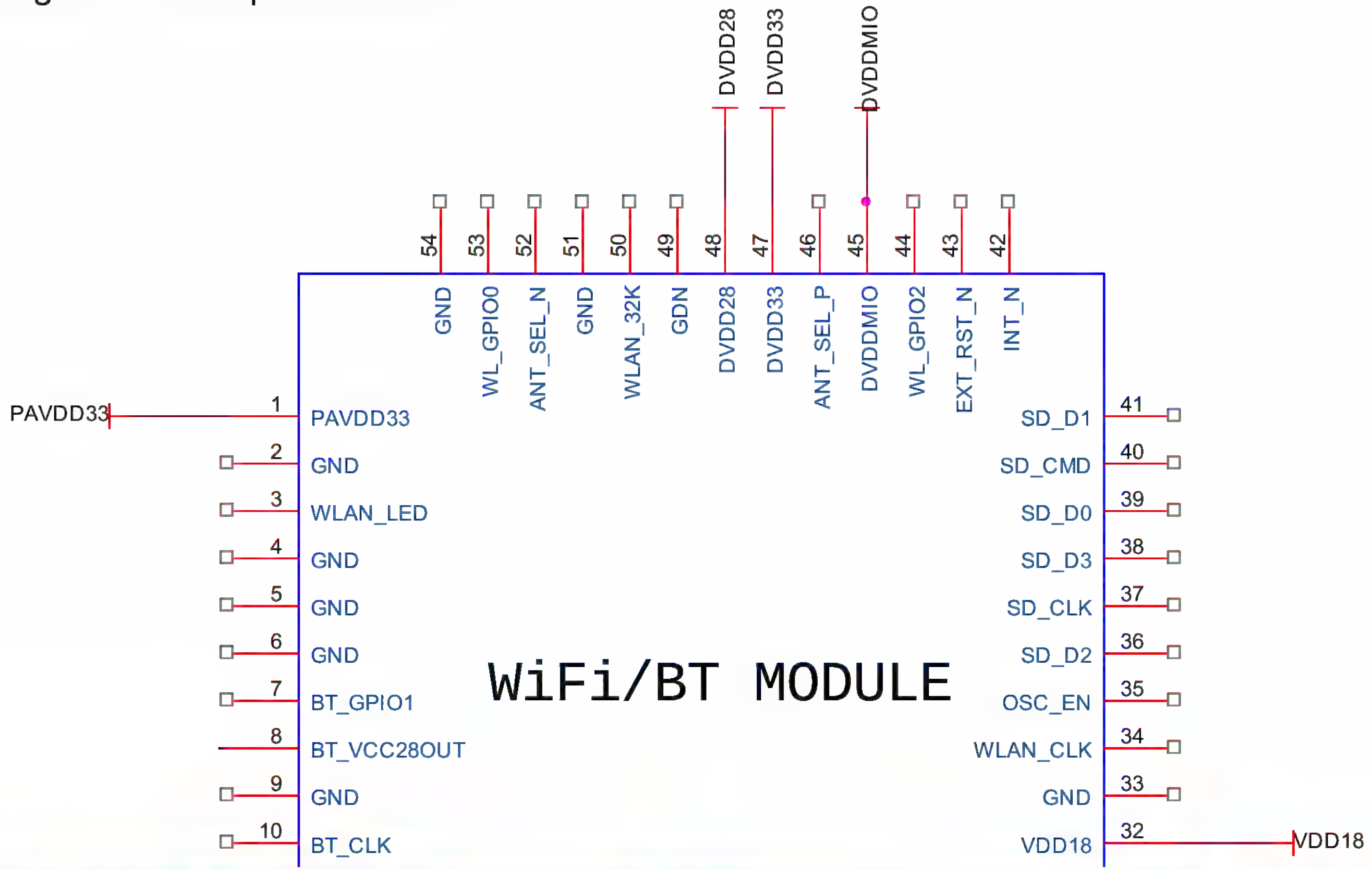
Schematic Design Guide(1)_Power Supply

- PAVDD33 is a dedicated input pin for module internal PA power supply and please connect it to 3.3V.
- DVDD28, DVDD33 and DVDDMIO are the WiFi portion digital IO power source, please connected to 3.0V for optimum Tx performance.
- VDD18 is the WiFi RF/analog/digital LDO input pin and can be connected to DC/DC 1.8V power source without degrading the module performance.



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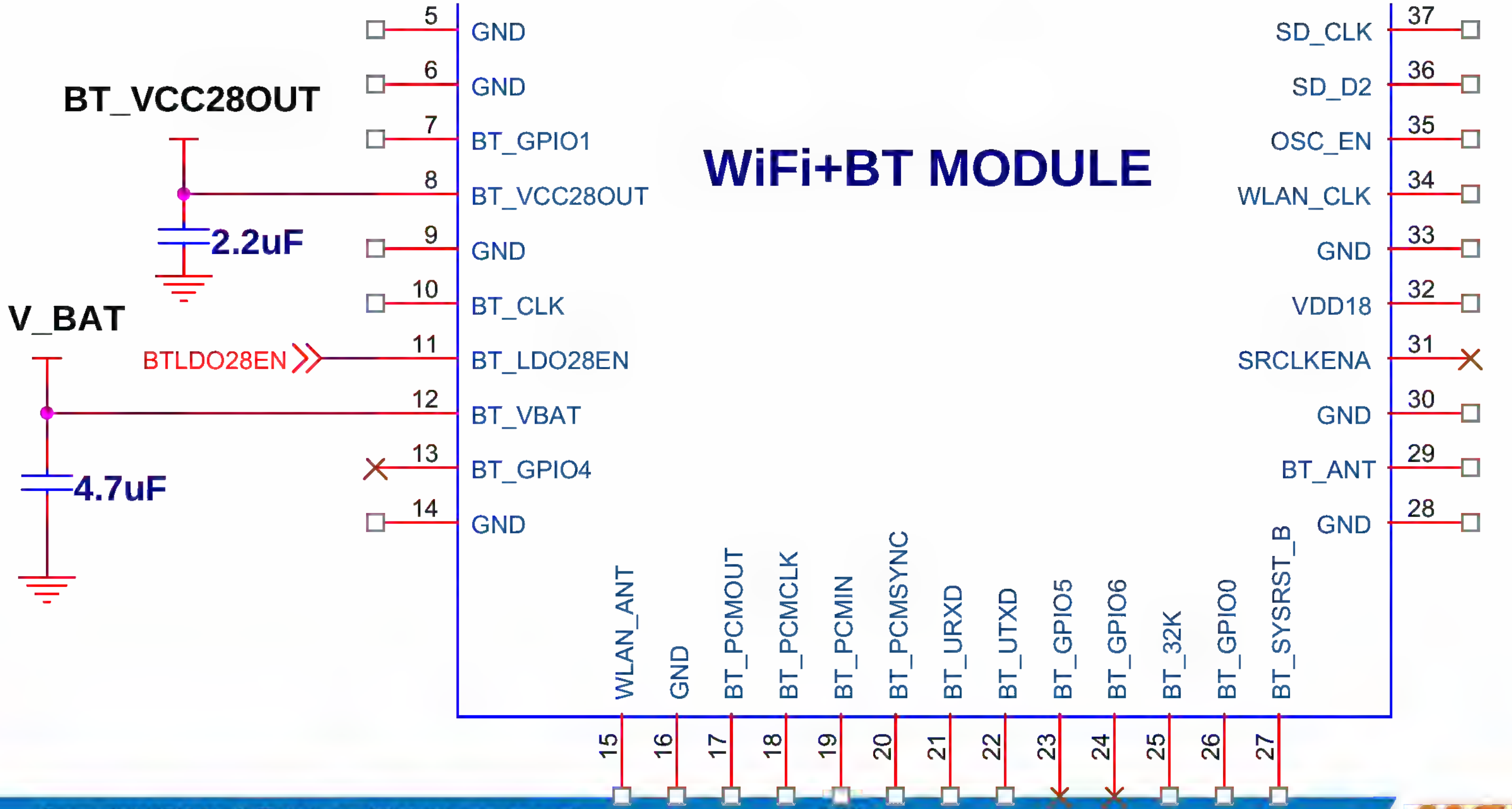
BT Power Domain (2)

- Distributed into two domains: V_BAT and 2.8V
  - V_BAT power source could come from phone battery and BT_VCC28 is the internal LDO output pin.
  - The BT 2.8V internal LDO was controlled by BTLDO28EN pin connected to host GPIO.



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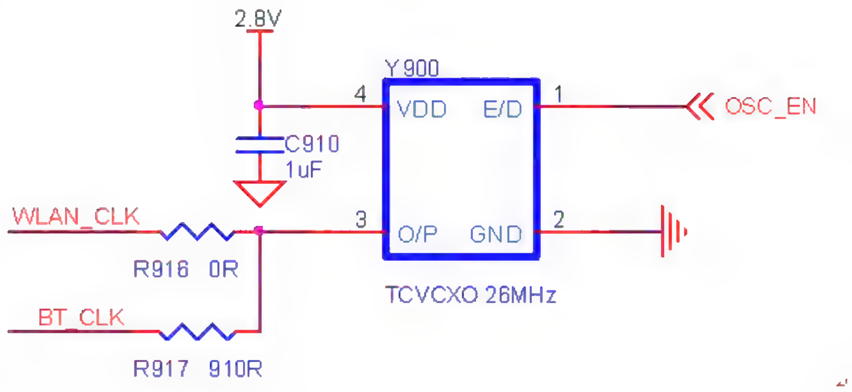
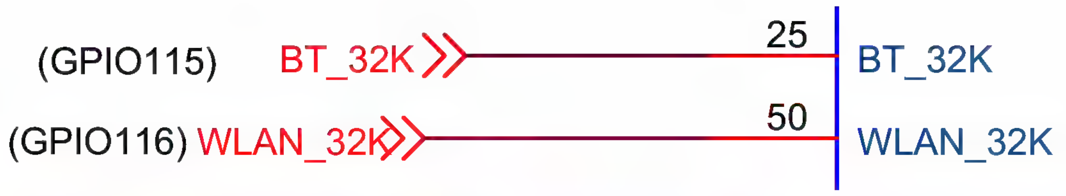
Schematic Design Guide(3)_Clock Source

- The WiFi/BT device can share a same clock with a daisy chain function .This mechanism allows Bluetooth can work normally without extra power consumption even WiFi operating in the sleep mode.
- The oscillator with 2.8~3.3V operated voltage , 20ppm tolerance and 15pF load capacitance is recommended



- 32KHz clock for device sleep mode
  - The 32KHz source come from BB GPIO output..



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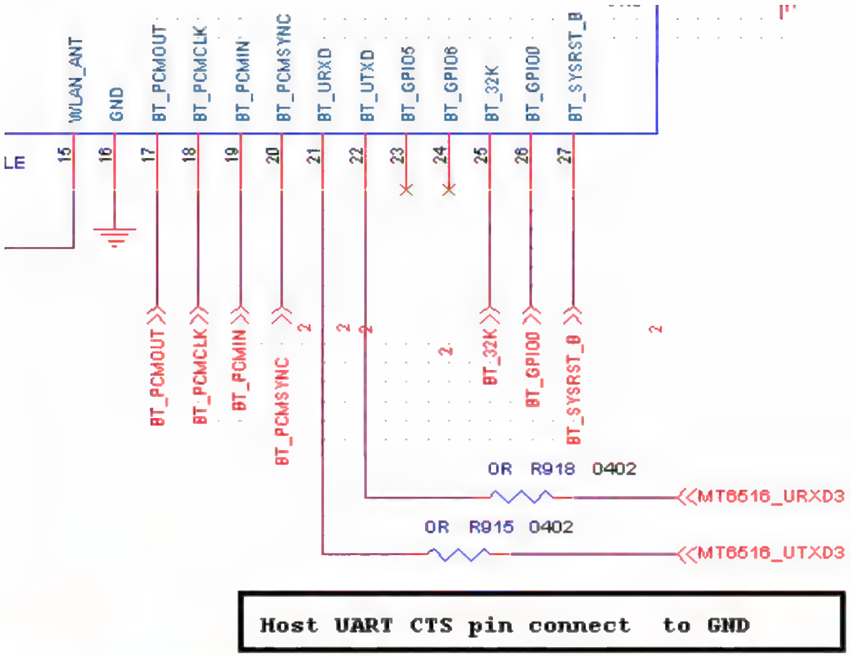
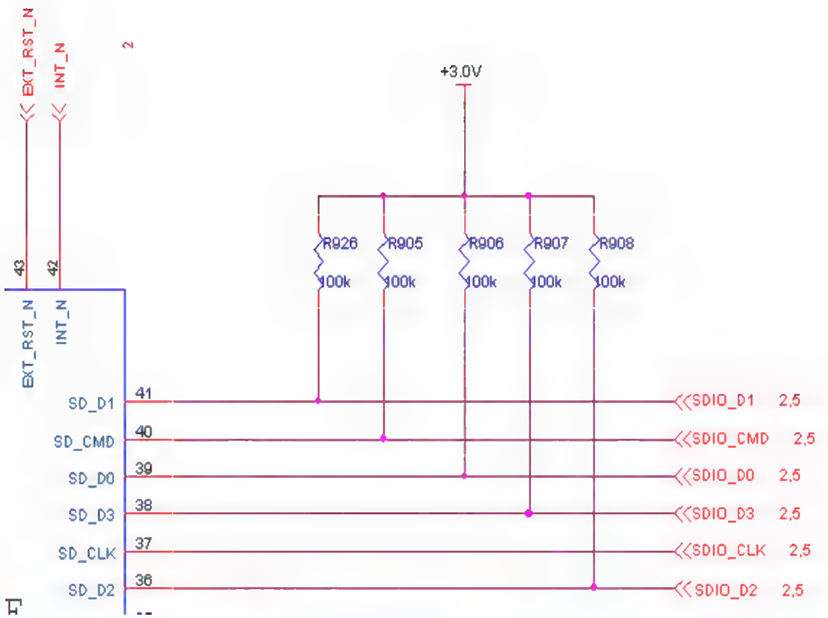
Schematic Design Guide(4)_Interface

- Please add 100K pull resistors for the SDIO data pin except SD_CLK pin.
- For BT UART interface, please note to connect the MT6516 host UART CTS pin to GND.

BT UART Interface



WiFi SDIO Interface



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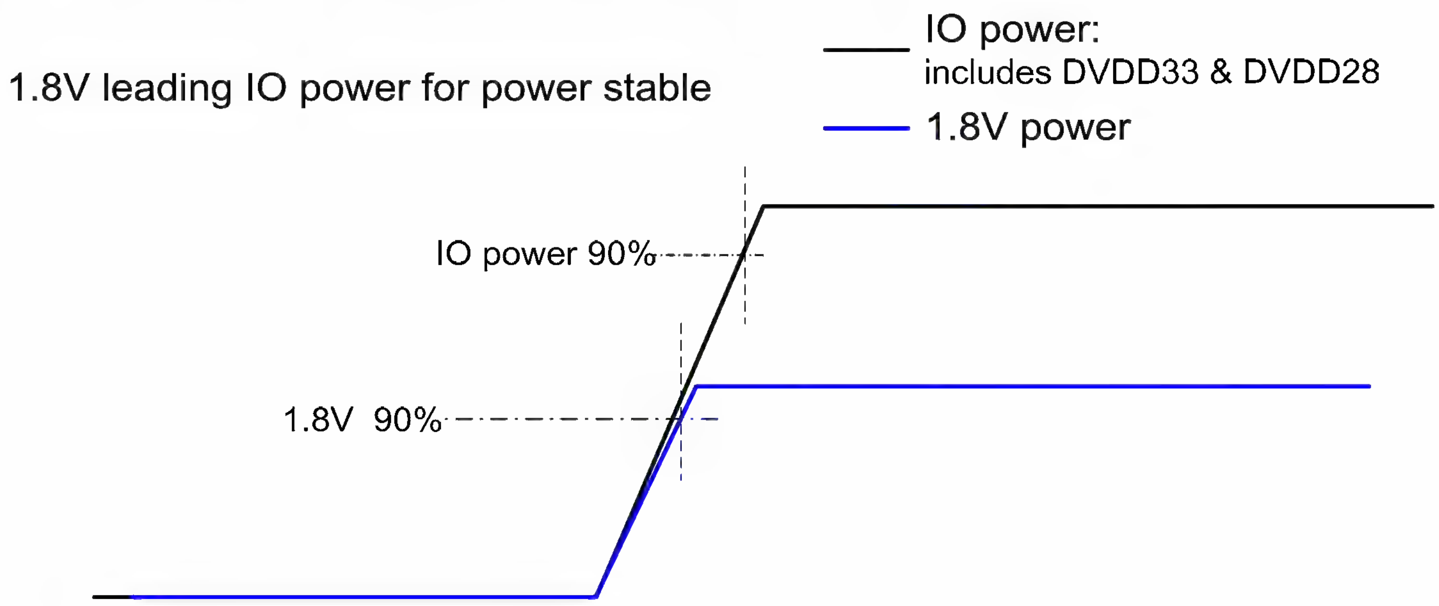
MT5921 Power Sequence



In order to prevent from the IO driving unpredictable signals, it is recommended that the 1.8V is applied before IO power or they are applied at the same time.

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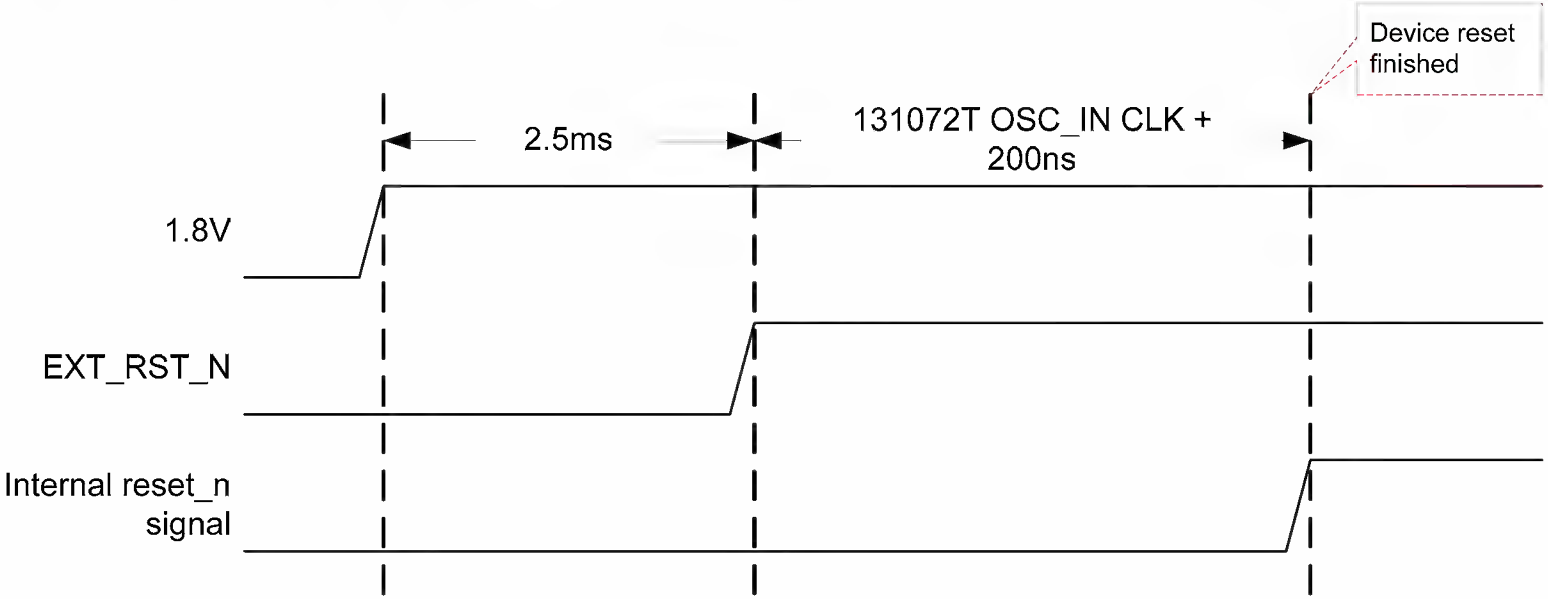
MT5921 Power On /Reset Timing



◆The power on reset time is related to the frequency of main reference clock source. The normal functions are not ready until the power-on-reset was done.

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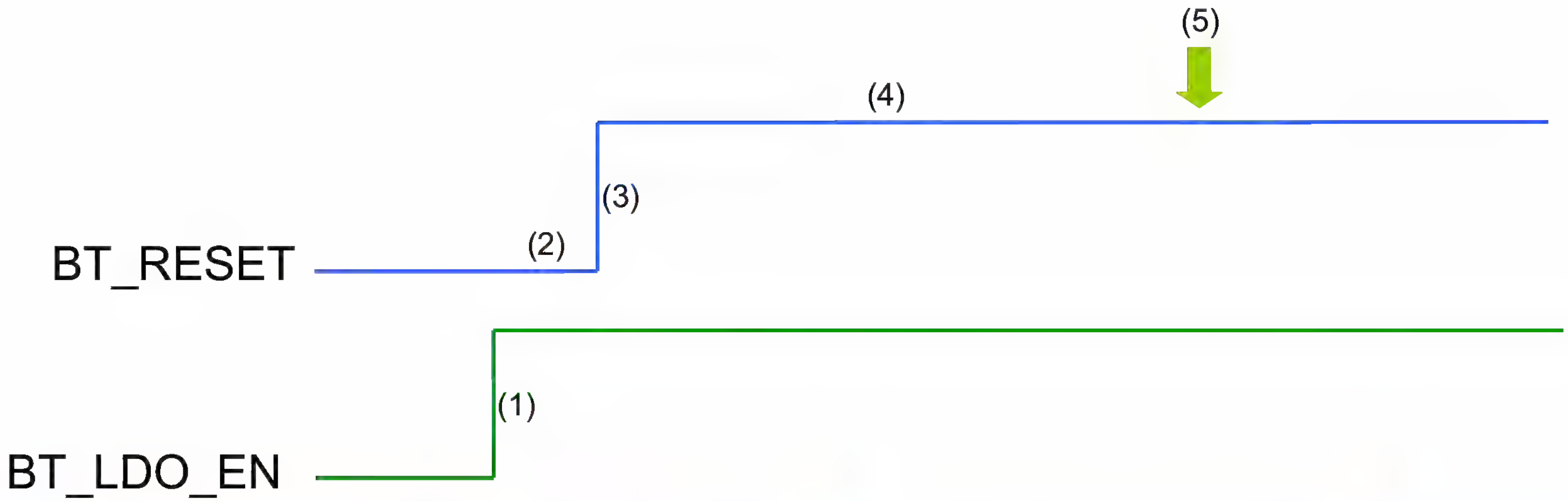
MT6611 Power On Initialization

- Hardware reset sequence & timing requirement
  - **(1)** Set **BT_LDO_EN** to high
  - **(2)** Wait for at least 2ms
  - **(3)** Set **BT_RESET** to high
  - **(4)** Wait for at least **1000ms**
  - **(5)** MT6611 is ready for receive HCI command



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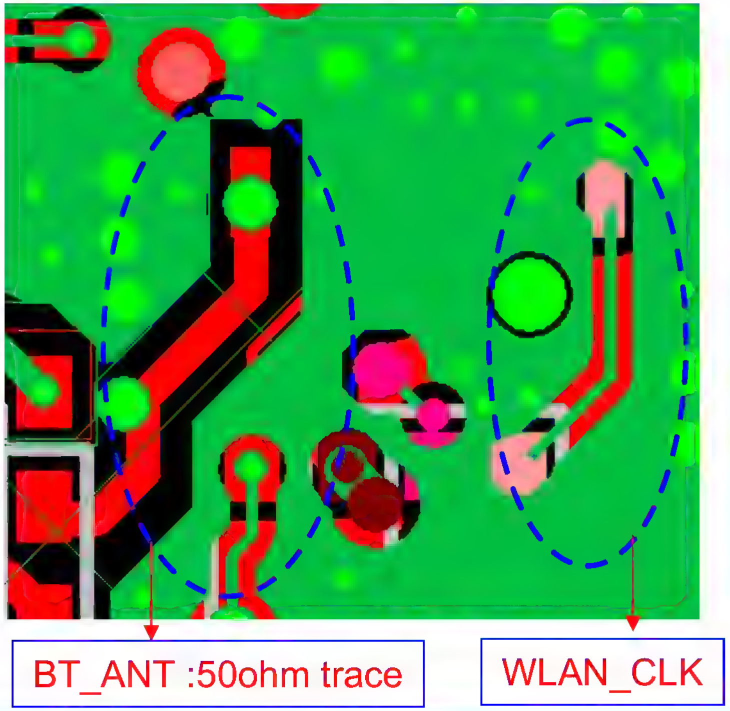
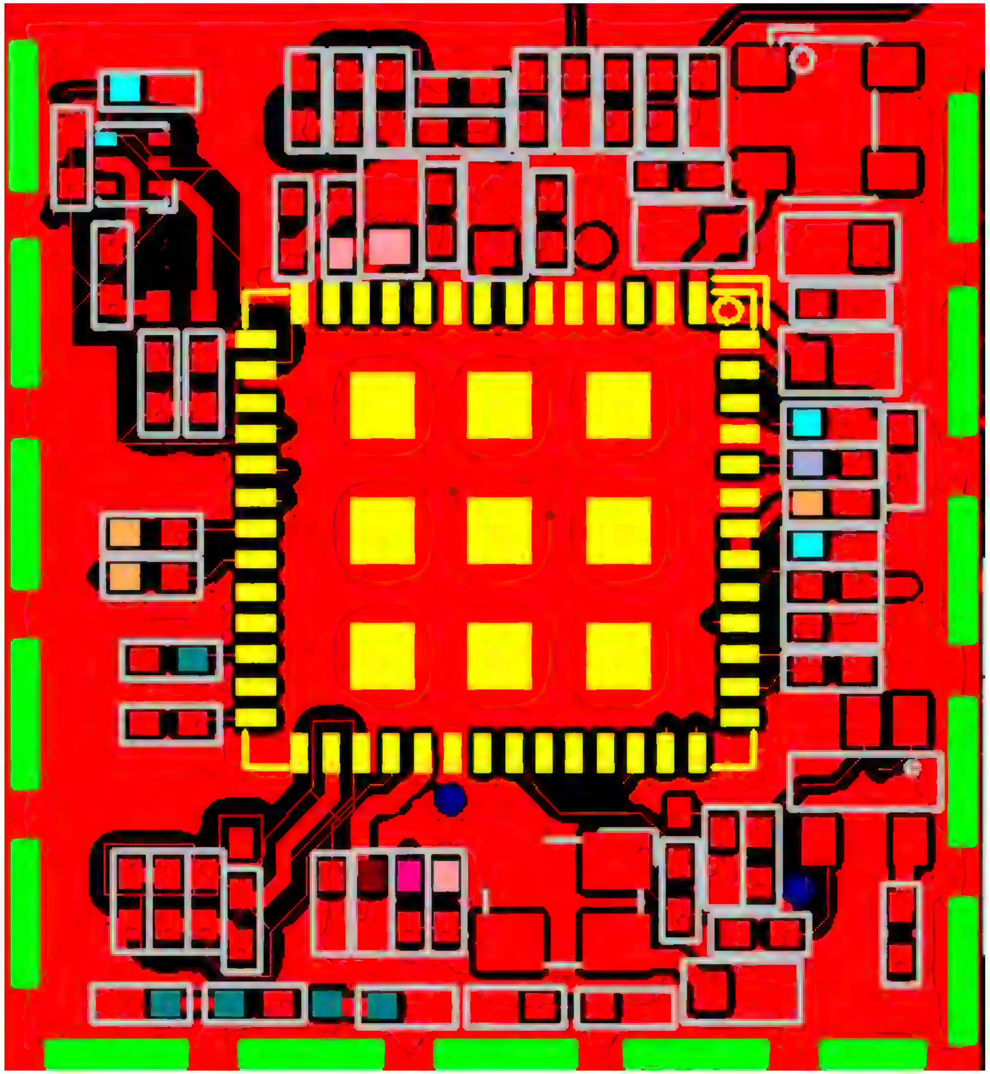
Module Layout Guide – 1/4

- Please place the bypass capacitors to the 3.3/2.8/1.8V power rail as close as possible.
- Please keep 50 ohm transmission for The WiFi/BT RF trace.
- Please isolate the WiFi/BT main clock trace with GND
- Please reserve the 9 square GND PAD for better performance for module



Layer1



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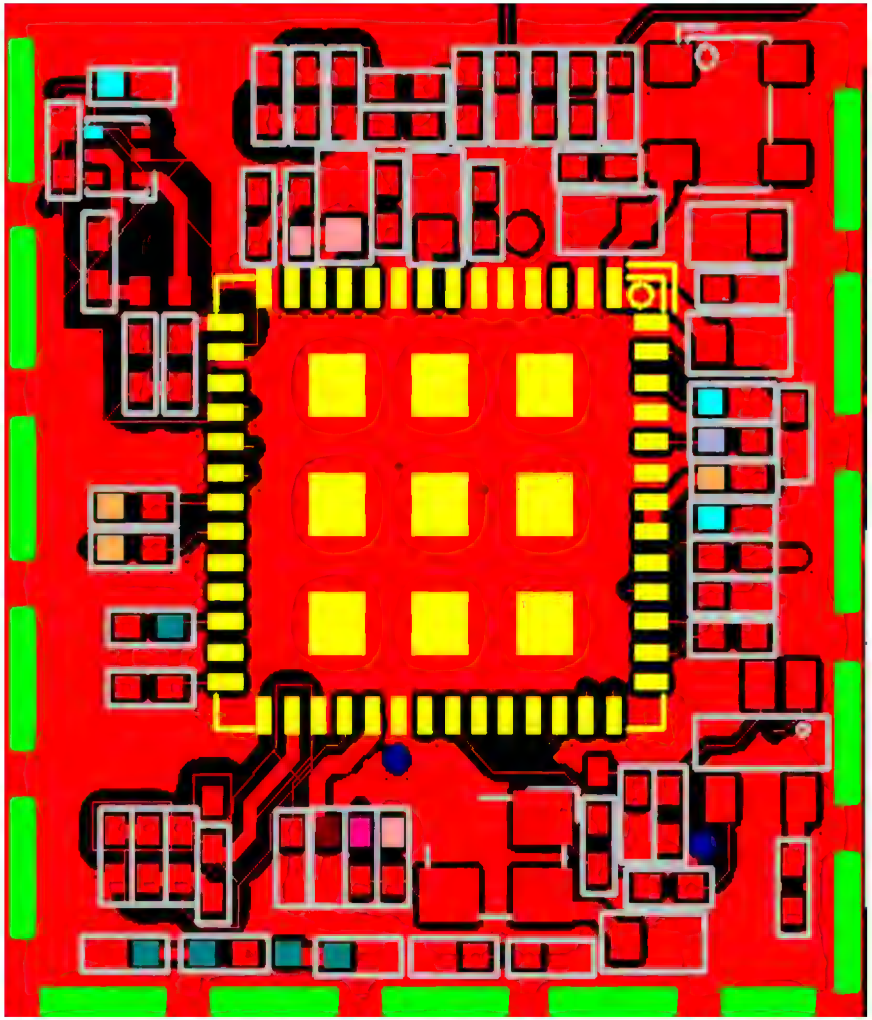
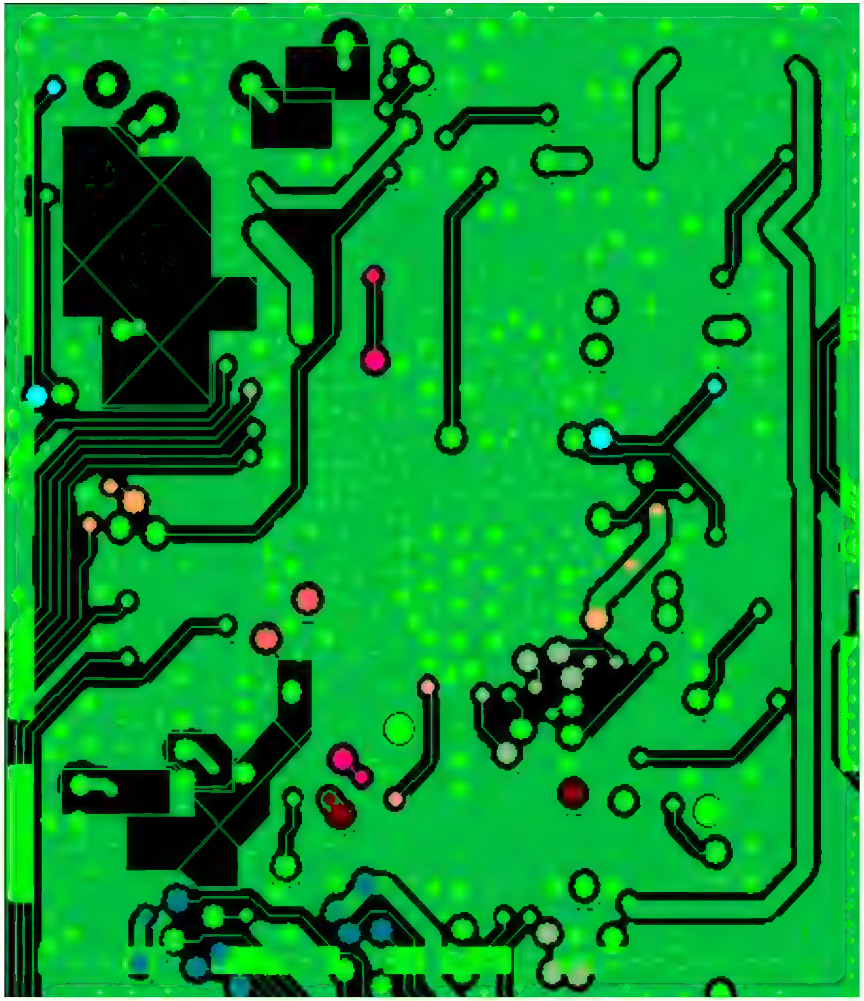
Reference Layout – 2/4

Layer1



Layer2



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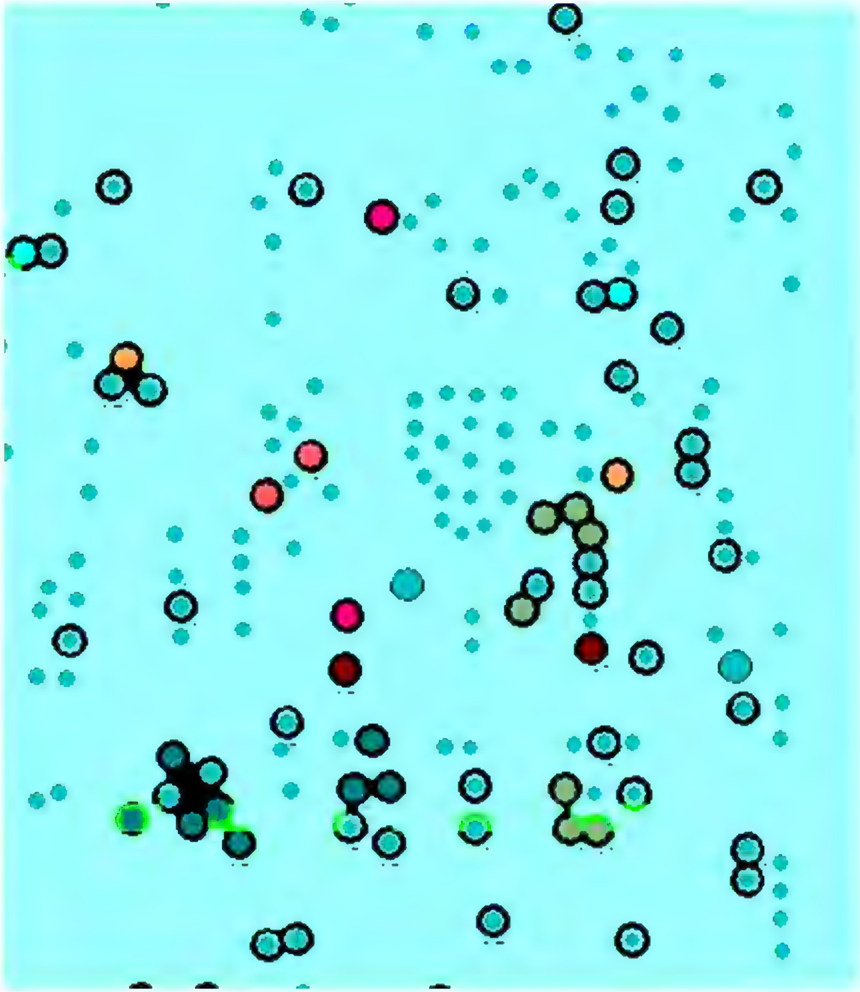
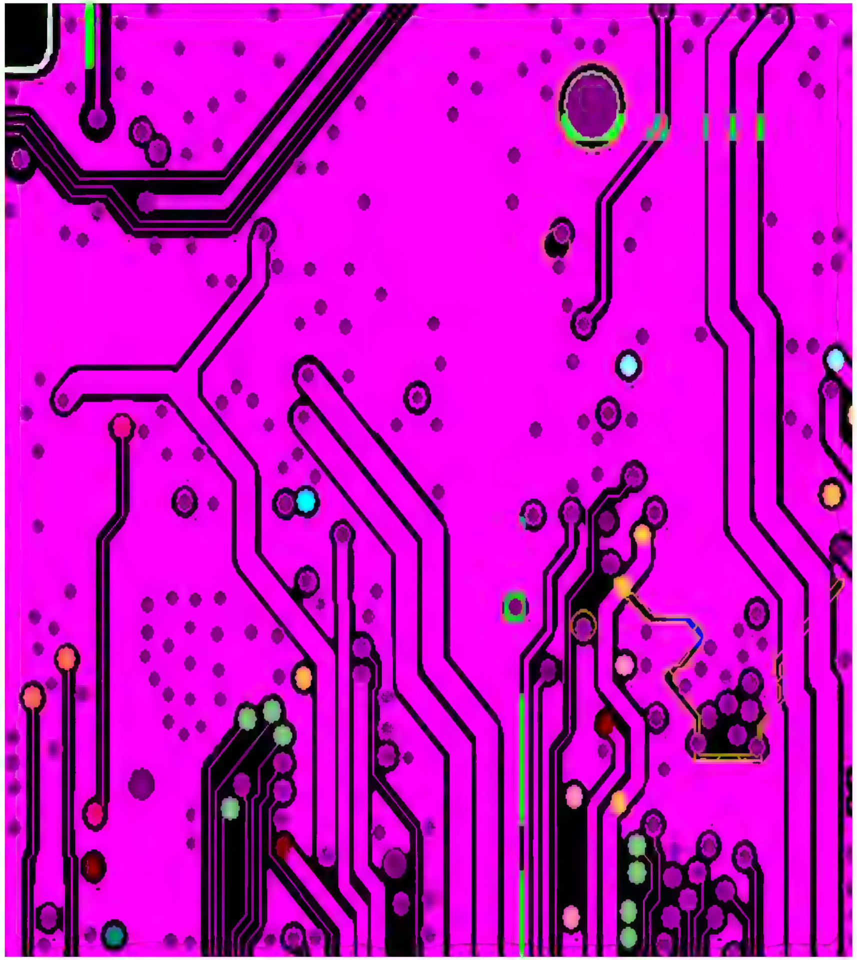
Reference Layout – 3/4

Layer3



Layer4



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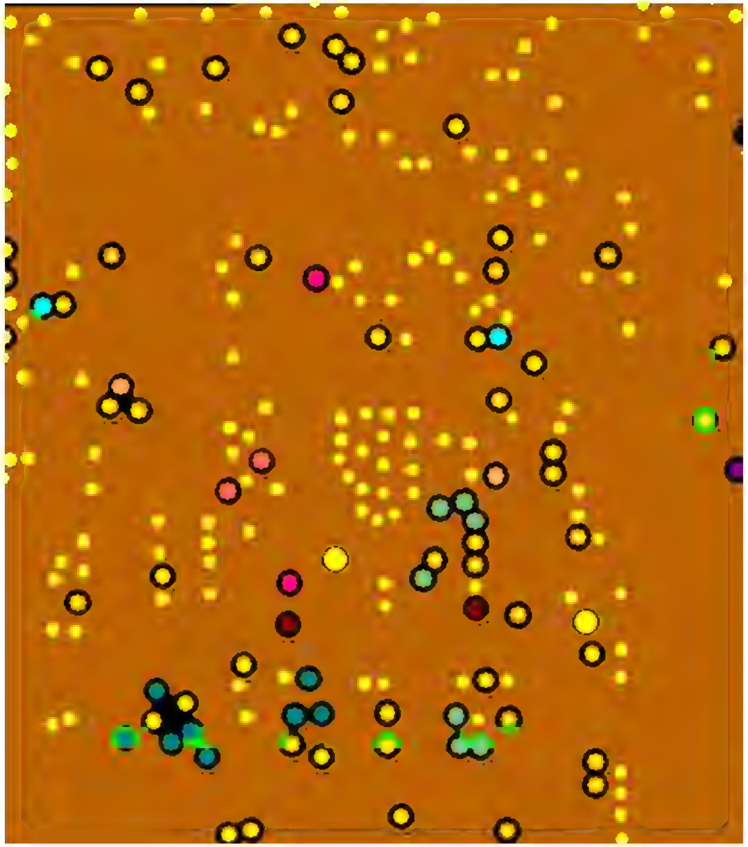
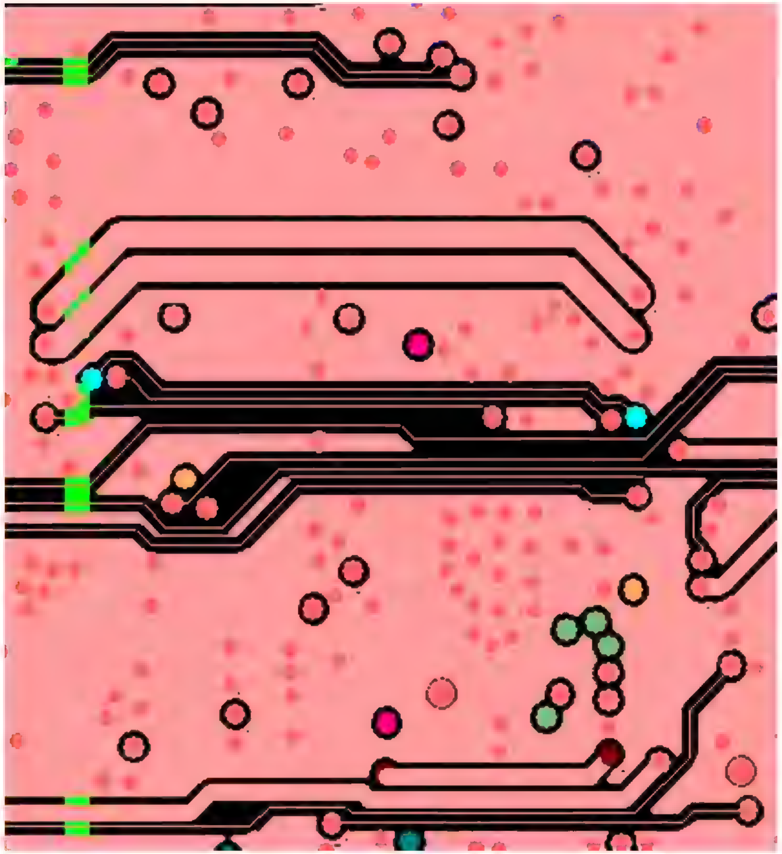
Reference Layout – 4/4

Layer5



Layer6



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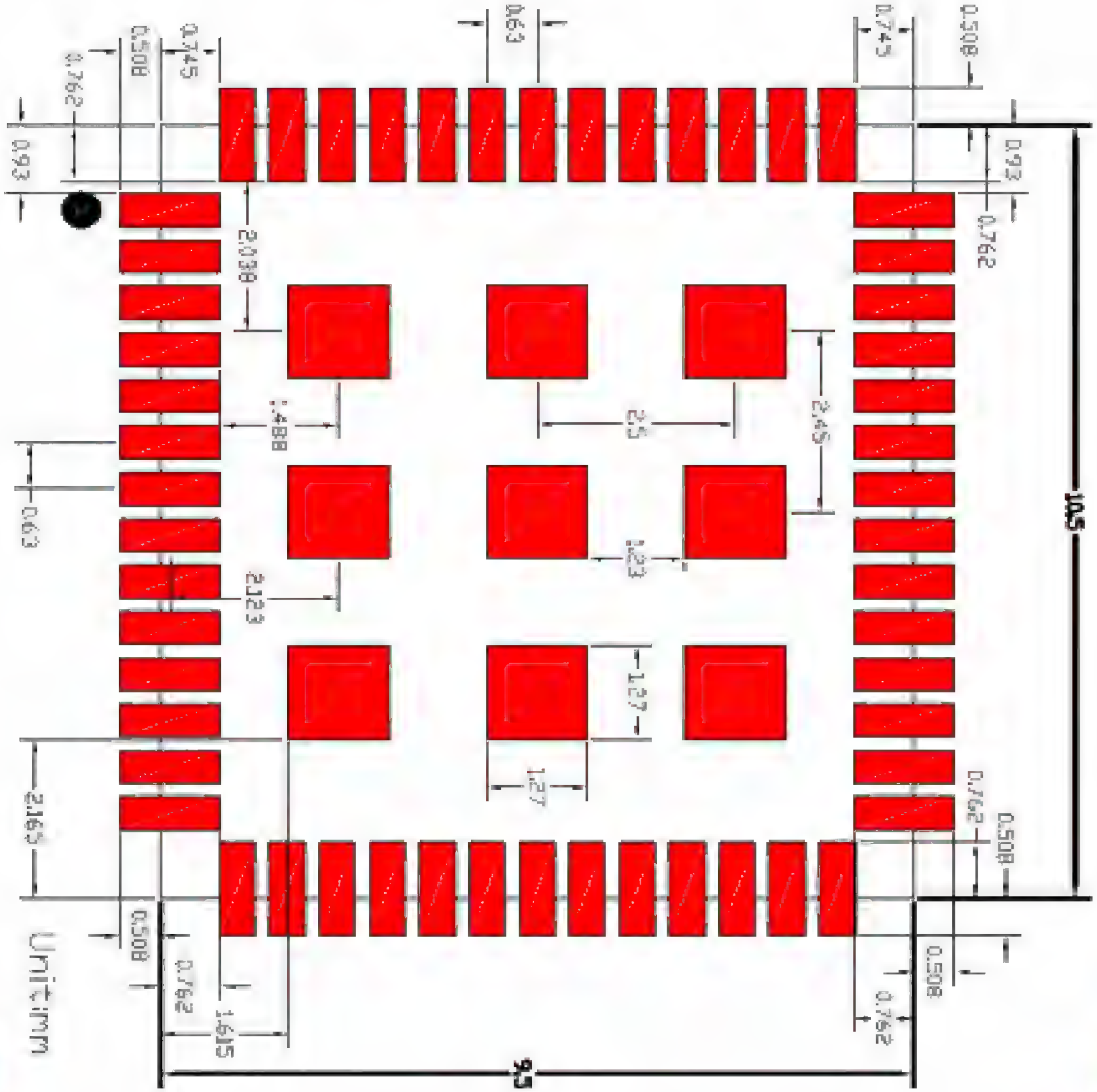
Module Footprint Layout Guide

Pin1



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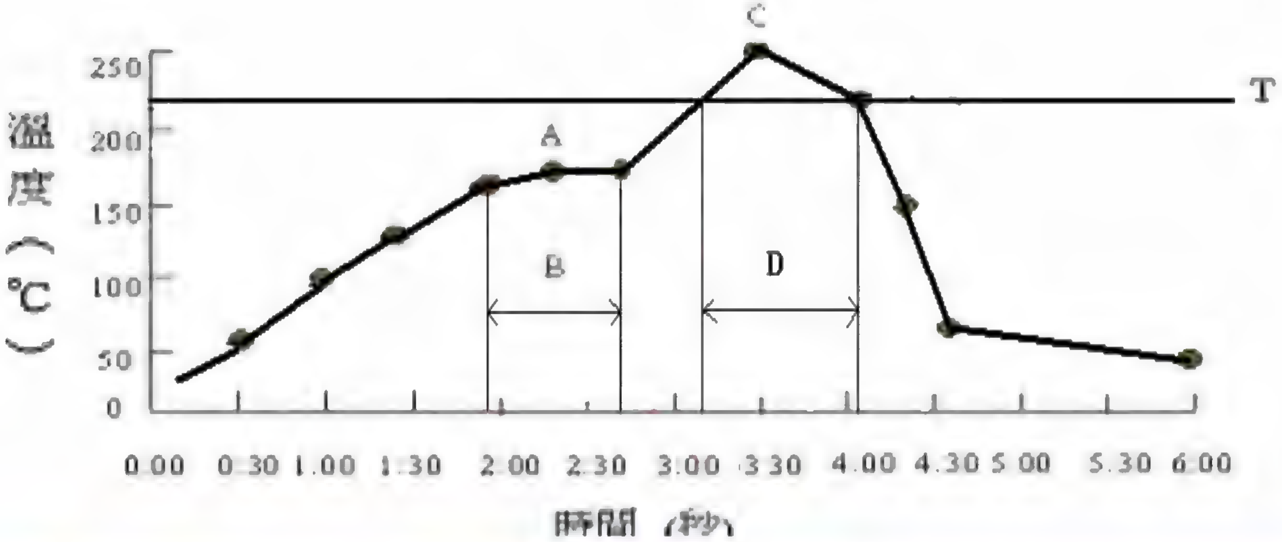
Module SMT Reflow profile

A. 預熱溫度 (PRE-HEAT TEMP.) C 最高溫度 (PEAK TEMP.)
B. 預熱時間(PRE-HEAT TIME) D: T ℃以上時間 (DWELL TIME AT T ℃ VARIABLE)

VARIABLES TYPE	A	B	C	D	T
LeadFree.rcp (AG4無鉛Sn/Ag4/Cu0.5)	180 ±10℃	40 ±10 sec	252 ±10℃	45 ±10 sec	220 ℃



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MT3326 Application Design Note

2009 / 04

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Agenda

- **MTK GPS Overview**
  - *MT3326 GPS Feature*
  - *MT3326 System Block*
- **MTK GPS Reference Design**
  - *MT3326 Schematic Design Note*
  - *MT3326 PCB Design Note*
  - *MT3326 QVL*
  - *MT3326 Debug SOP*
  - *MT3326 ATE Tool*
- **MTK GPS Tier One Performance**
- **Summary**
- **Q&A**

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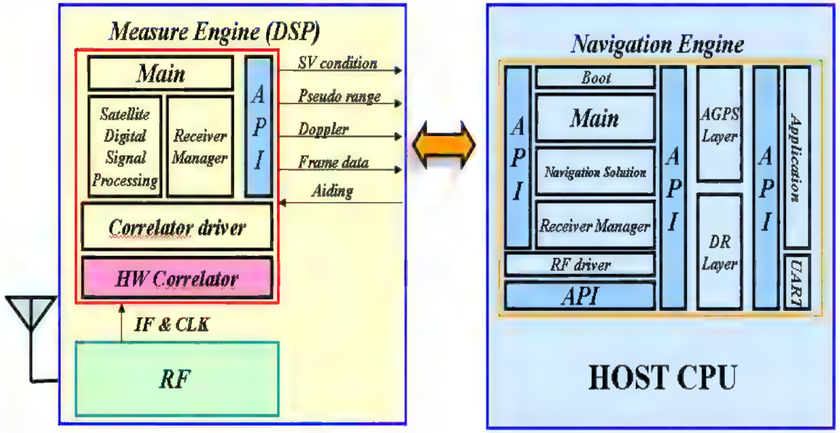
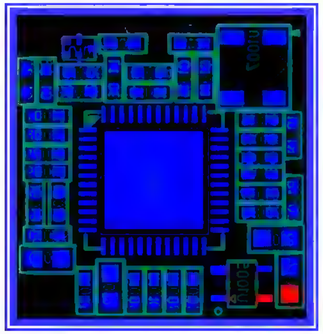
MT3326 Features

- **Dimensions:**
  - 48-pin QFN lead-free package (6 x 6 x 0.85 mm)
- **Specification:**
  - Host-based GPS receiver
  - 22 tracking/66 acquisition channel GPS receiver
  - Supports WAAS/EGNOS/MSAS/GAGAN
  - Supports up to 210 PRN channels
  - Jammer detection and reduction
  - Indoor/outdoor multi-path detection and compensation
  - Supports A-GPS with FCC E911 compliance
  - Maximum fix update rate up to 10 Hz
- **Reference Clock Support:**
  - TCXO Frequency : 12.6 MHz ~ 40.0 MHz
- **Interfaces:**
  - 2 UARTs , SPI , I²C , GPIO
- **Low Power Consumption:**
  - Acquisition mode : 39 mA
  - Tracking mode : 26 mA





Compact Layout Area : 12 x 12 mm

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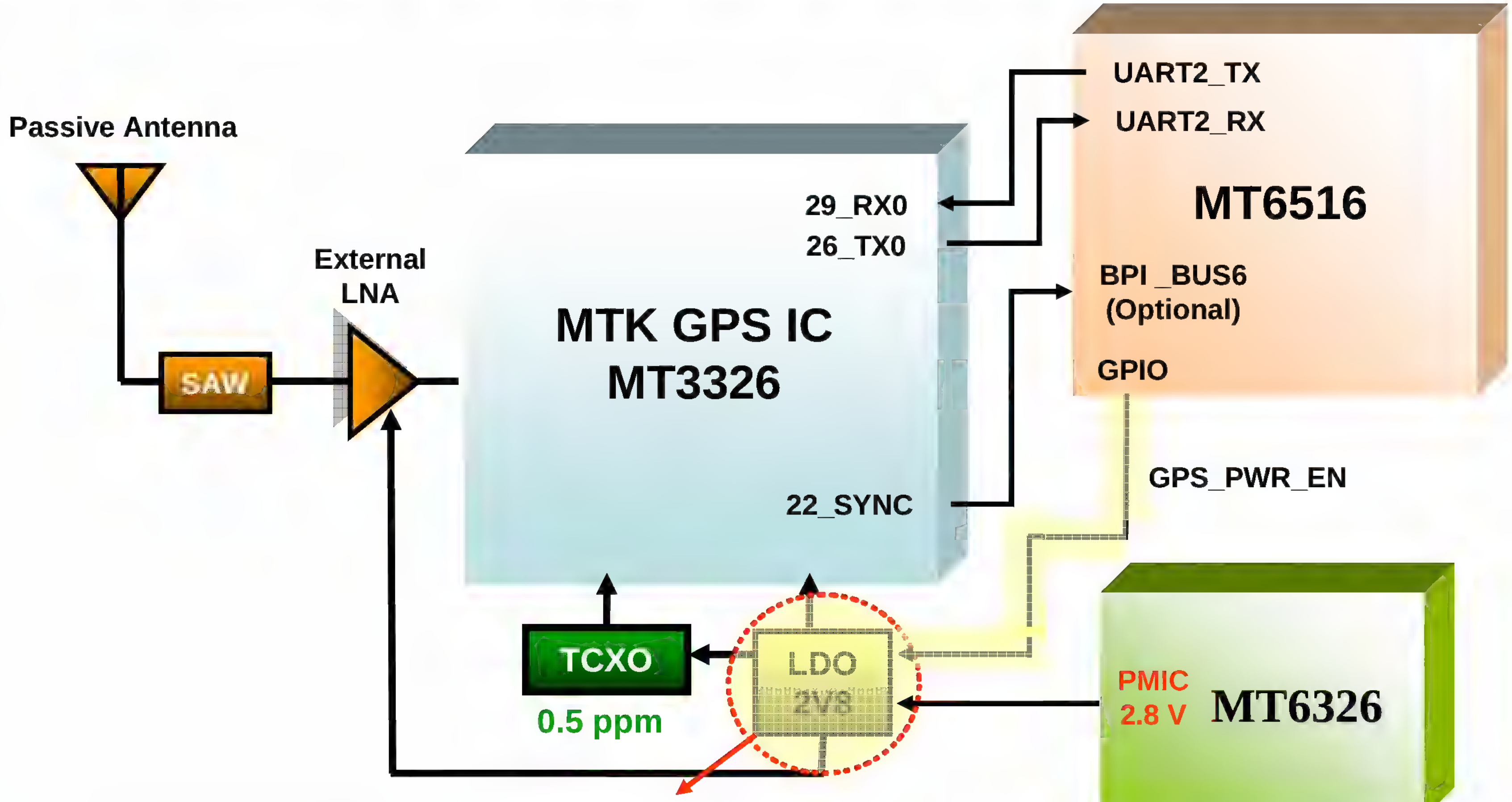
MT3326 Functional Blocks



Optional: If 2.8V voltage can be provide by PMIC, the external LDO can be eliminated.

- GPIO Pull Low → GPS Receiver Off
- GPIO Pull High → GPS Receiver On

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MTK GPS Reference Design

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MTK GPS Phone Total Solution

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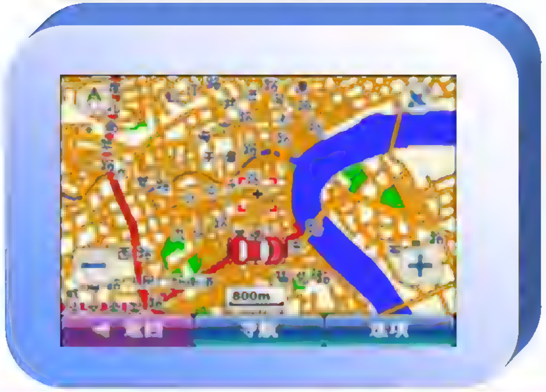
GPS Antenna Review

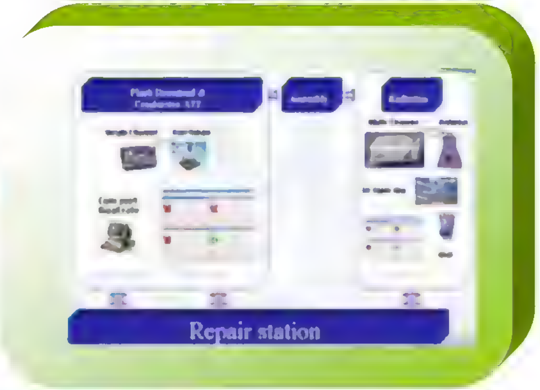
Reference Design

Tier-1 Field Trial

MTK GPS SW Build in



Factory Tool Support



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MT3326 Reference Circuit

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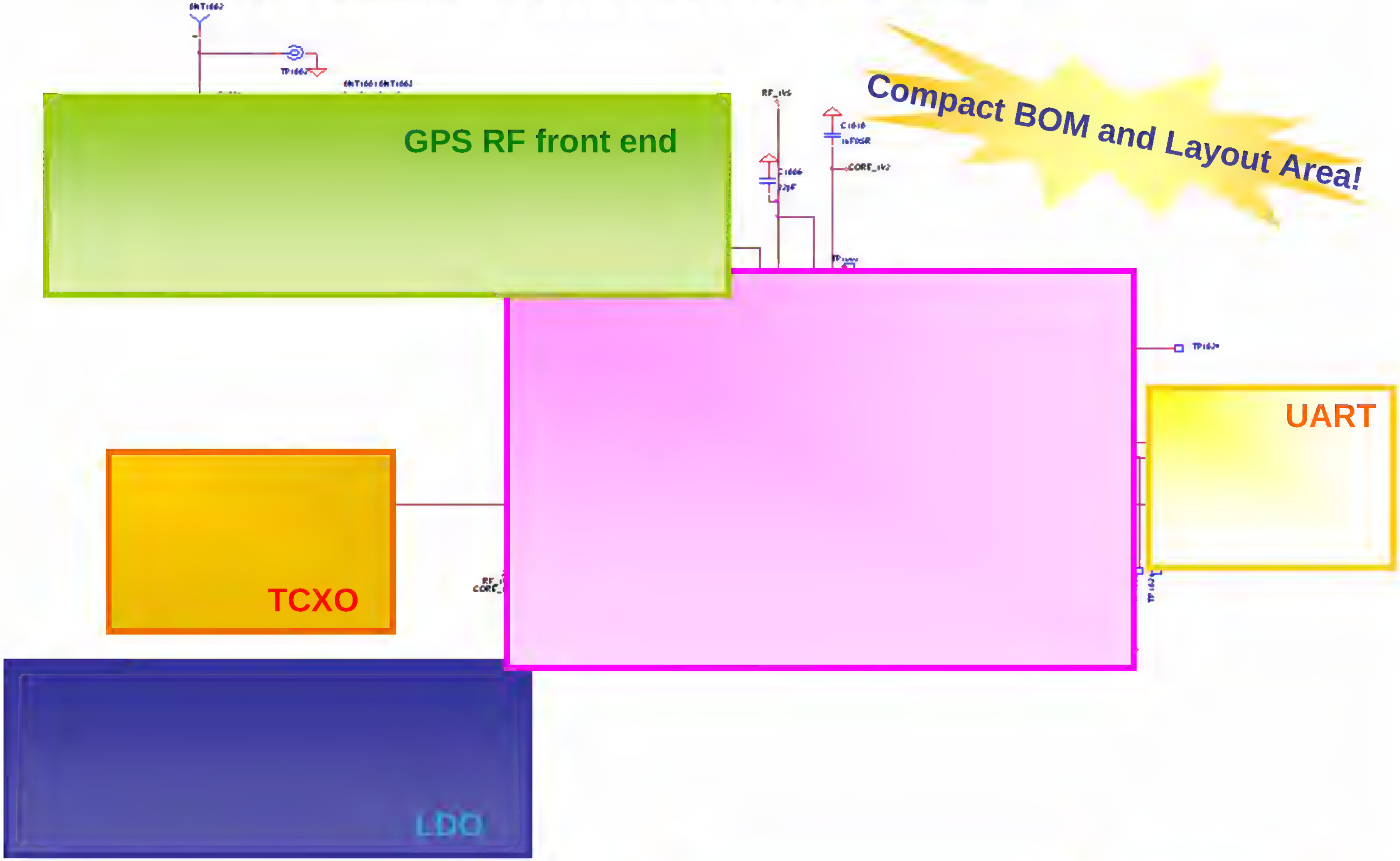

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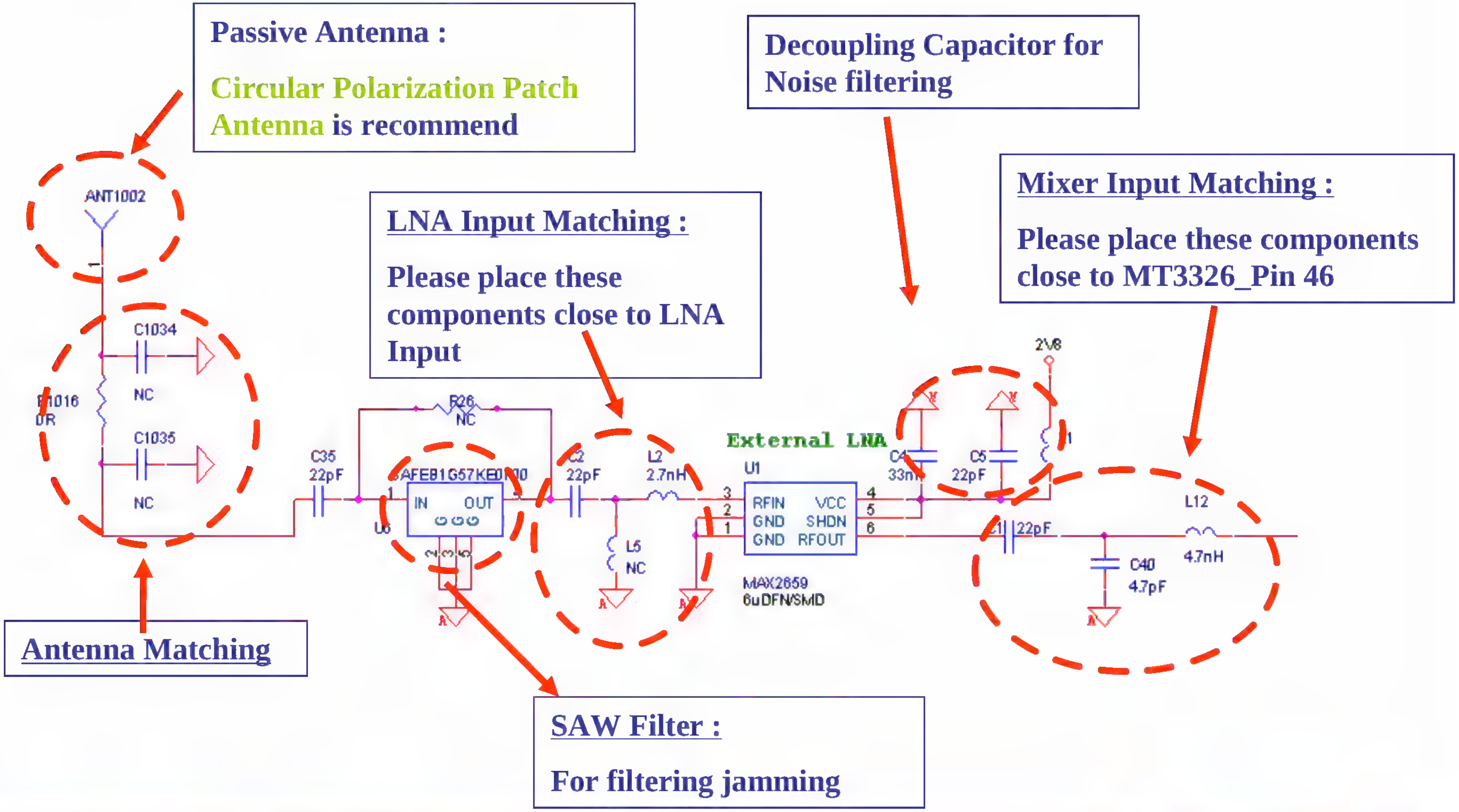
MT3326 Reference Circuit (2/4)

GPS RF Front End



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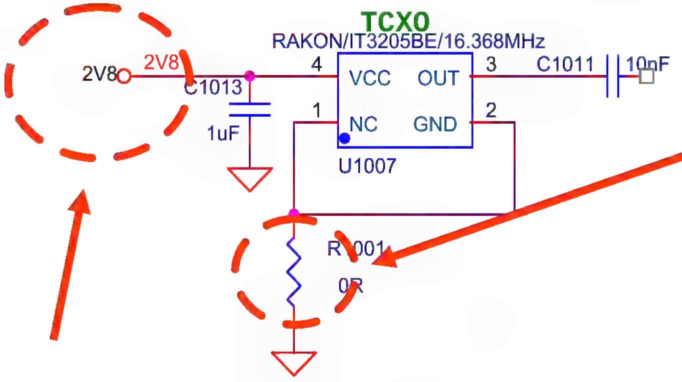
MT3326 Reference Circuit (3/4)

TCXO

Frequency :16.368 MHz

Frequency Stability : +/- 0.5ppm



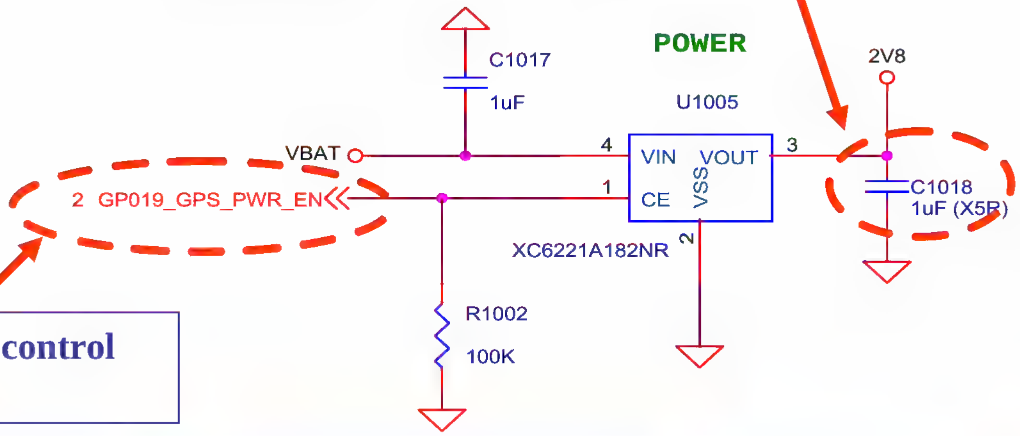
Reserve 0 ohm to isolate the impact of PCB GND temperature variation on TCXO.

TCXO VCC :

Avoid the noise interference for frequency stability

Stabilize the LDO output Voltage

LDO



GPIO from MT6516 to control LDO On/ OFF

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MT3326 Reference Circuit (4/4)

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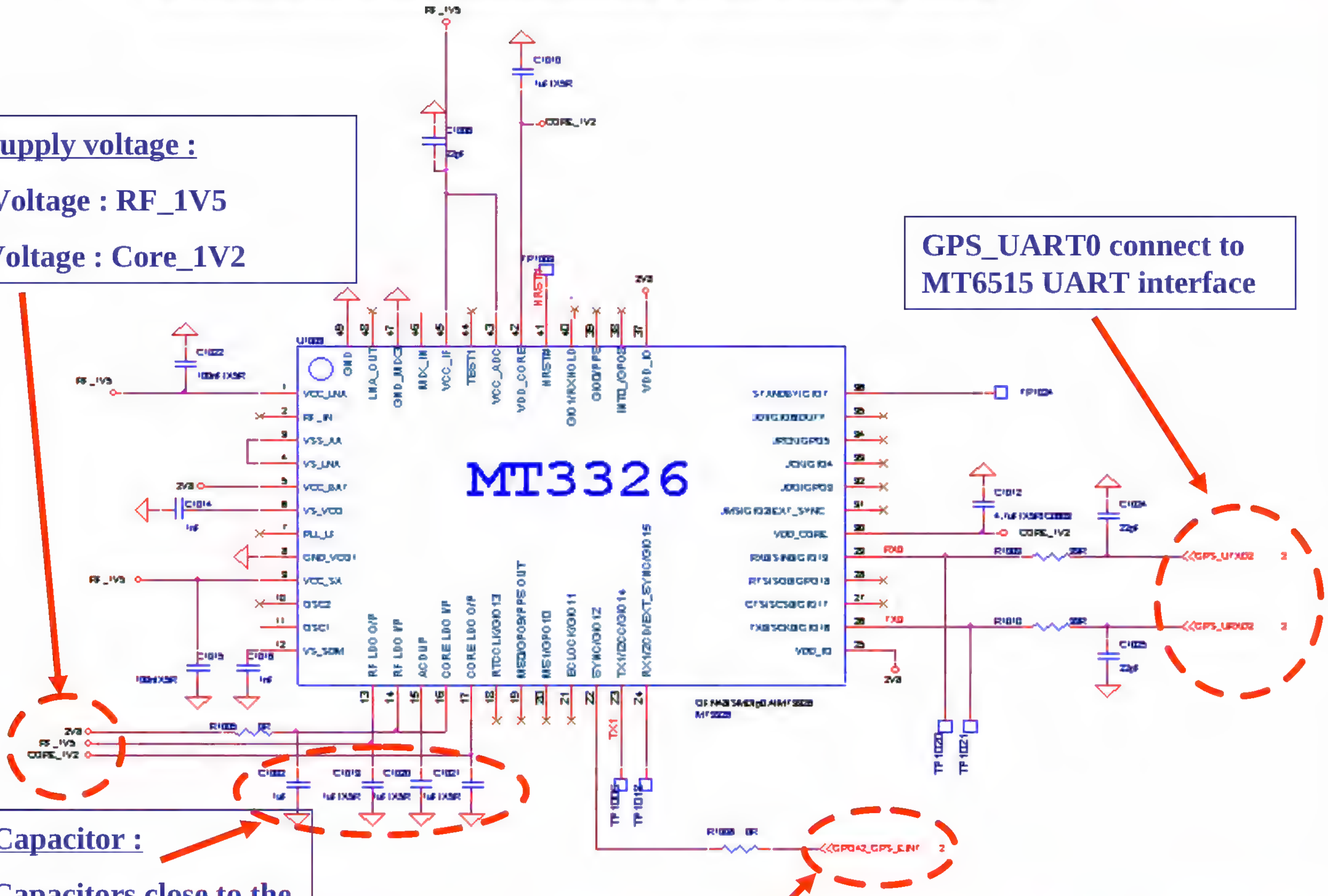
MT3326 Supply voltage :

*Analog Voltage : RF_1V5

* Digital Voltage : Core_1V2

GPS_UART0 connect to MT6515 UART interface



LDO I/O P Capacitor :

Place these Capacitors close to the MT3326 LDO input Pin and output Pin for stabilizing voltage

Optional : Connect to MT6516 BPI_BUS.

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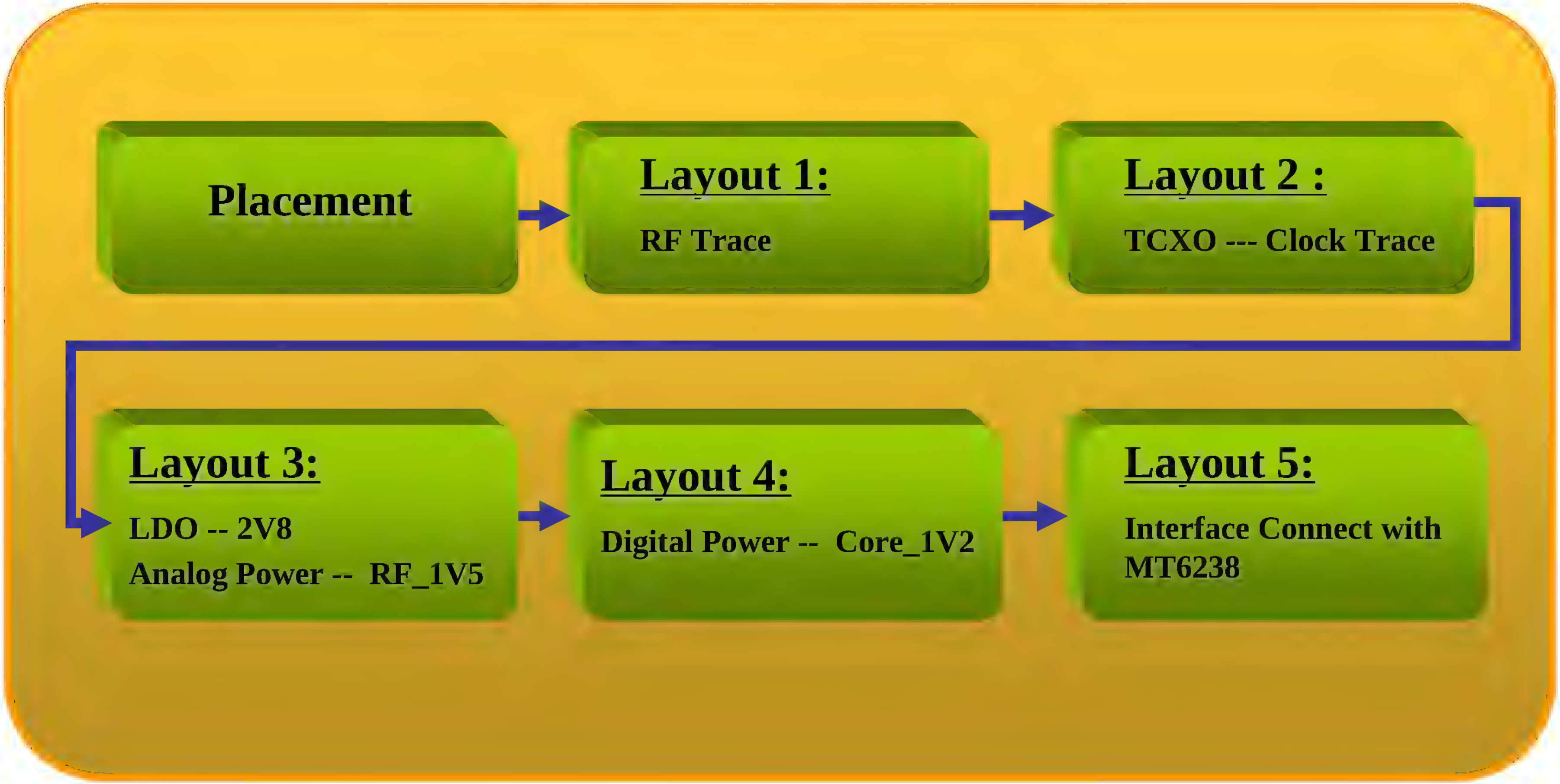
PCB Design Flow



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PCB Component Placement (1/3)

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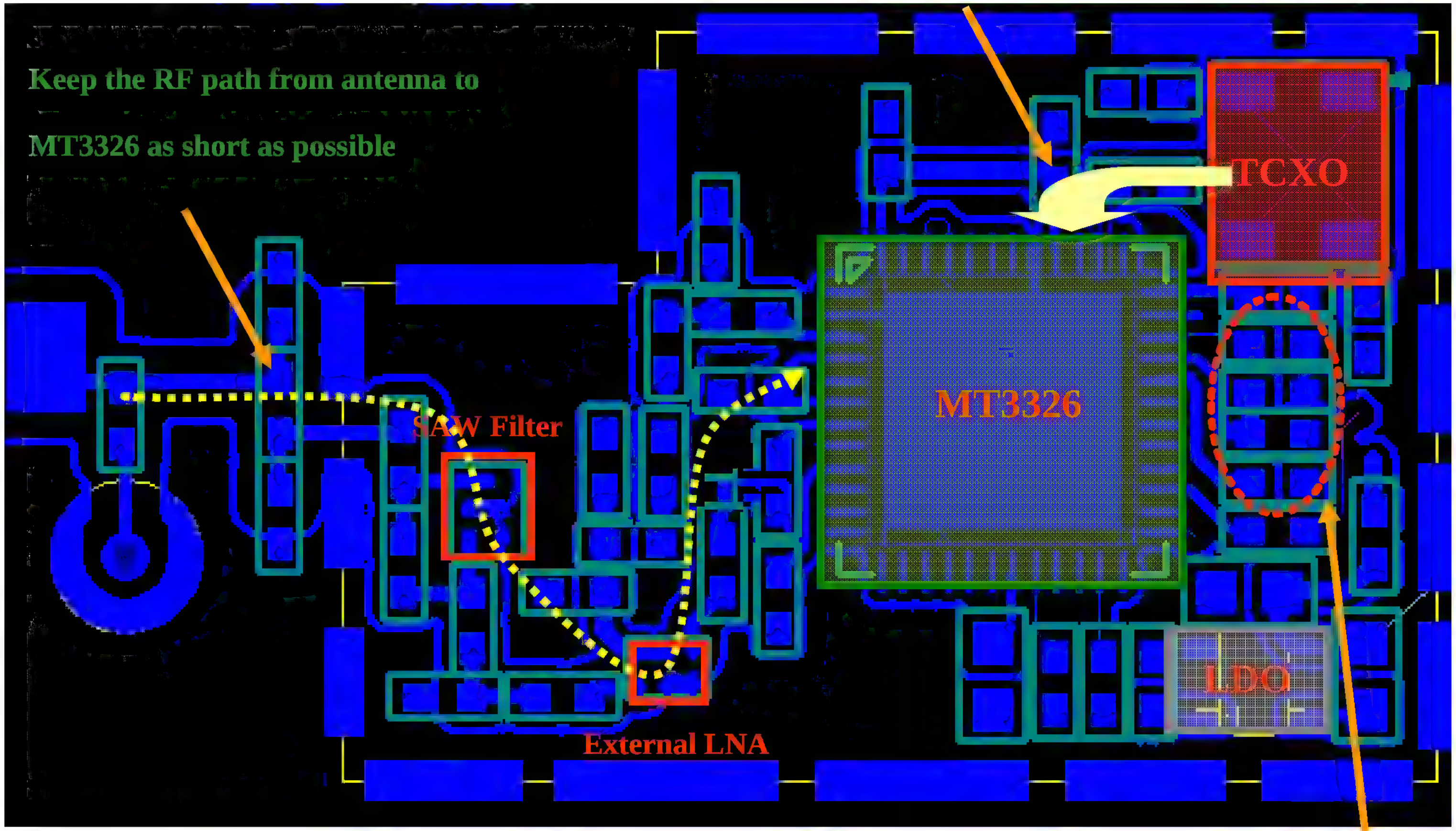
The route of reference clock is the shortest to avoid interfering by other noise



The Capacitors close to analog and digital voltage output

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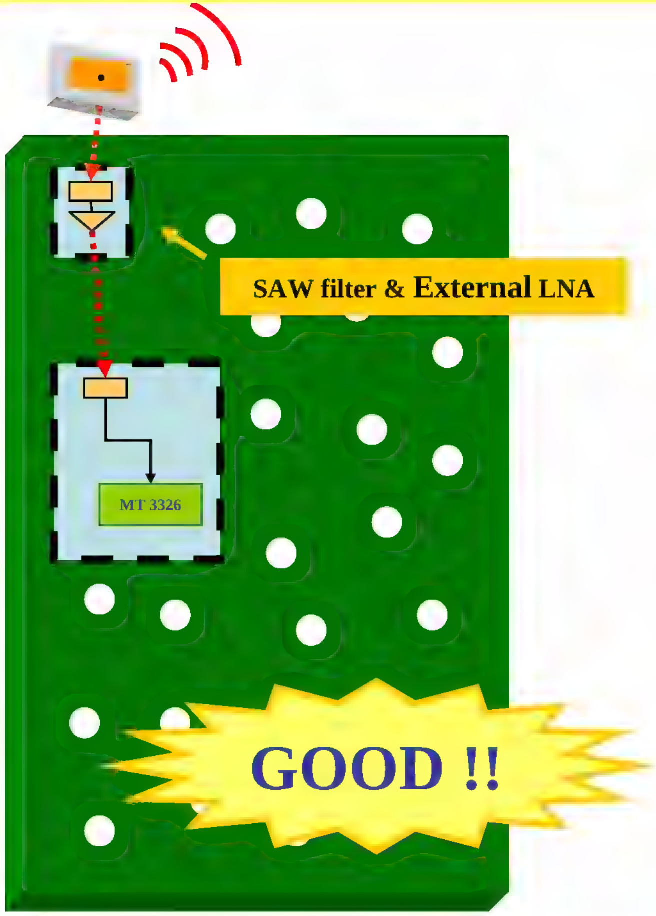
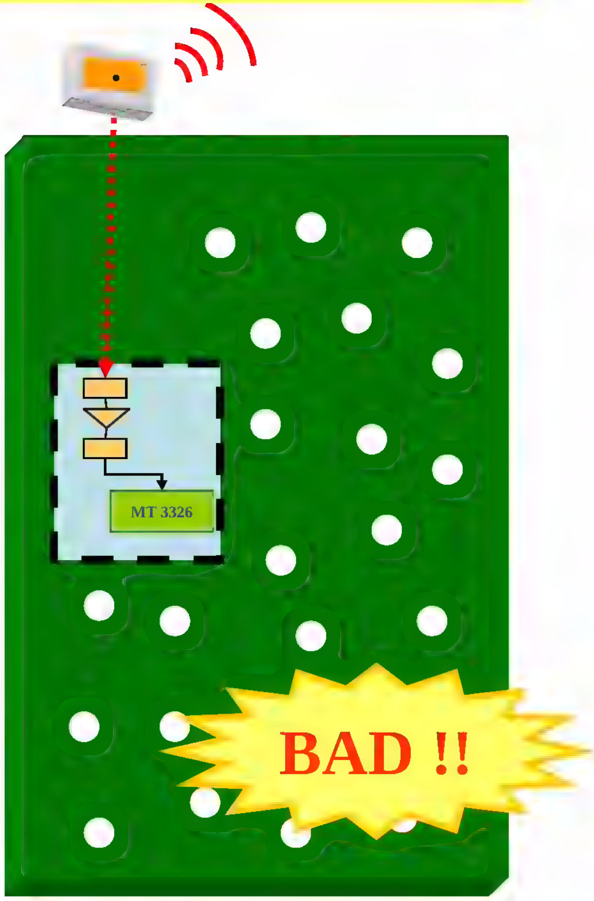
PCB Component Placement (2/3)

If the location of GPS function block is far away from GPS antenna Pad, please place the first-stage SAW filter and external LNA close to GPS antenna port for reducing RF path loss.





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GPS Antenna Placement (3/3)

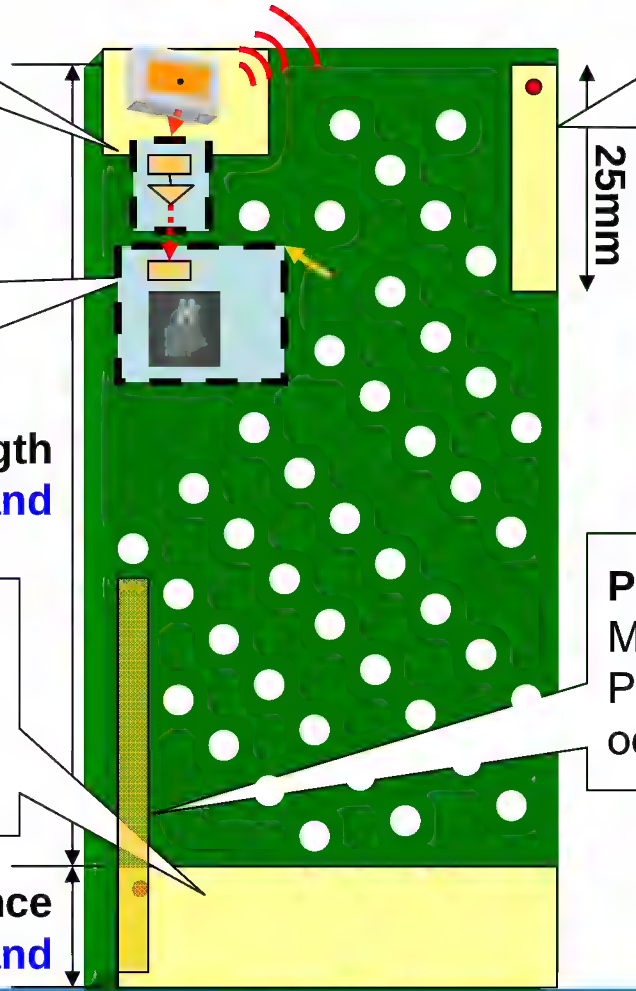
GPS Antenna
12X12X7 Active Patch

GPS Placement
10.5mmX10.4mm
Near GPS Antenna

90mm GND Length
for triple band

GSM Antenna
Metal monopole on bottom.
Avoid GSM TX interfere with GPS RX.

15mm clearance
for triple band



BT Antenna
Metal PIFA is recommended.
It can be mounted on Speaker Holder. Chip antenna is also an option.

Pen
Material is **plastic** near GSM ANT.
Place GSM Cal Kit below pen. It occupy less GSM ANT Area.

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Proposal of GPS Patch Antenna for Slim Phone

- **Probe-Feed RHCP Patch (Fig.1)**
  Patch Size: 12X12X4, 13X13X4
  Vendors: Whayu, Yageo, CIRO, Microgate, Amotech

- **Probe-Feed LP Patch (Fig.2)**
  Patch Size: **15X10X4, 16X6X5**
  Vendors: Whayu, Yageo, CIRO, Microgate, Amotech

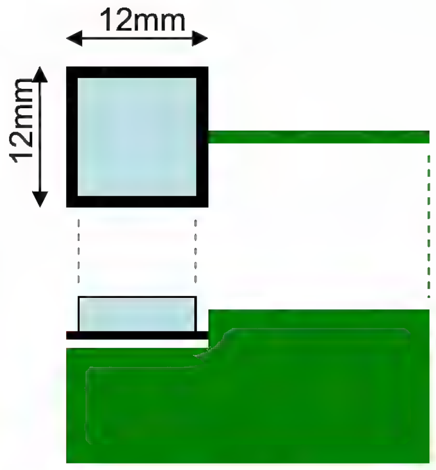

Fig.1

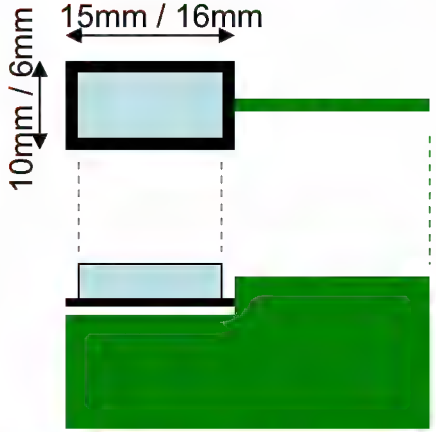

Fig.2

12X12X4 | 15X10X4 | 16X6X5

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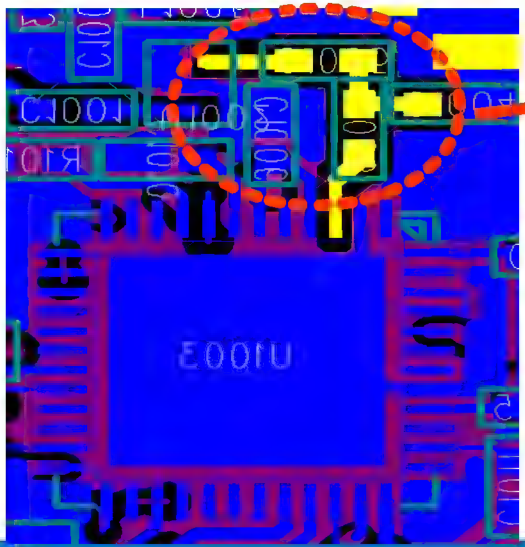
PCB Layout Design Note (1)

- **RF Part :**
  - RF Path keep as short as possible for reducing RF signal transmitted loss.
  - All RF traces have to do impedance control (50 Ohm) for good sensitivity.
  - RF traces route on the surface layer and far away from other high speed signal trace are recommended.
  - Isolate external LNA input and output pin by copper plane.
  - To keep the digital signal trace far away from the GPS layout area.
  - Clear the metal below all matching component area to reduce the parasitic capacitance.



Clear the metal below the RF trace and Pad !!!

High Parasitic capacitance couldn’t reach optimal RF match

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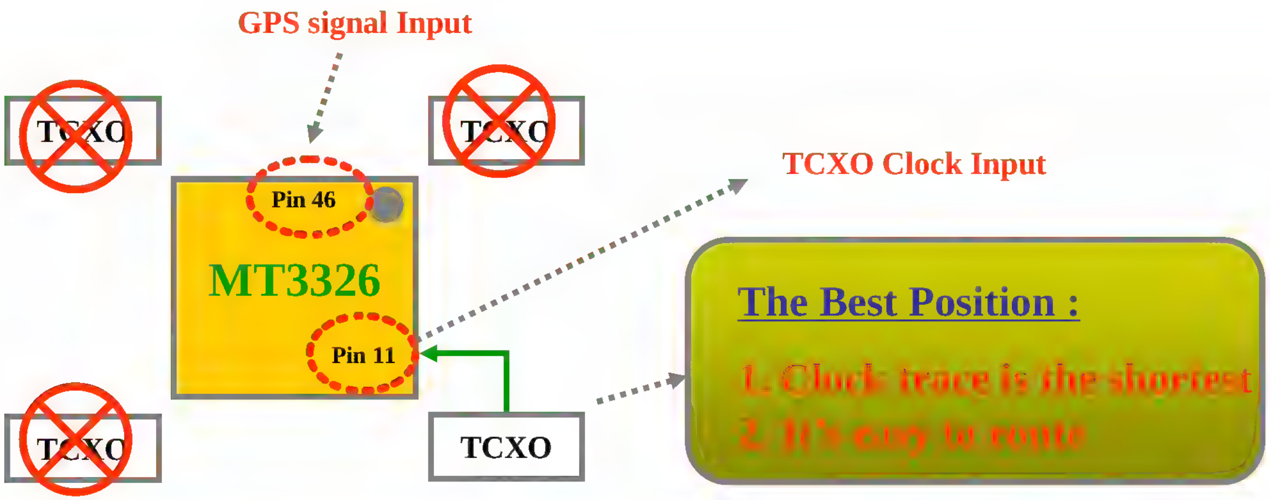
PCB Layout Design Note (2)

- **TCXO Part:**
  - **Keep TCXO clock trace as short as possible.**
  - **Keep the noisy traces far away from TCXO clock traces.**
  - **TCXO clock traces enclosed by PCB copper is recommended.**
  - **Position TCXO far away from any high temperature component like as GSM_PA to avoid the frequency drift.**



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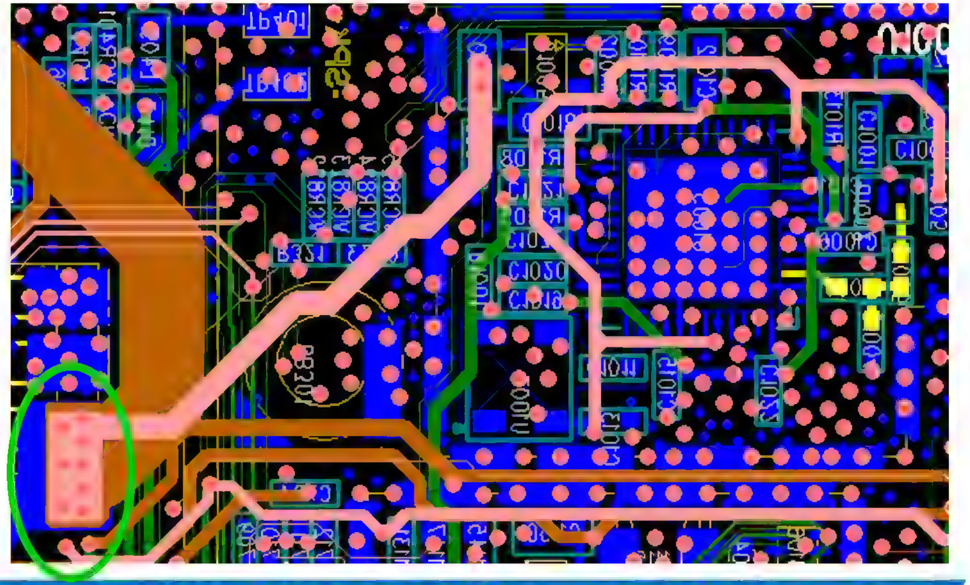
PCB Layout Design Note (3)

Power Line Part

- Power trace should keep as low impedance and adequately add de-coupling capacitor for noise filtering.
  - Recommended width of power trace : Main Trace: 20 mils at least
    Branch into IC pin/ball: 10 mils at least
- Keep de-coupling capacitors close to the power pin of GPS chipset and external LDO.
- Use many, many via holes to connect the power traces between layers.

Use many via holes to connect the power traces between layers



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Qualified Vender List -- TCXO

Component	Part number	Manufacturer	Vendor
TCXO (16.368 MHz) +/- 0.5ppm	IT3205BE/IT3205CE	Rakon	Aurum Tech Inc.
	TTS14NSB-A8	TEW	Unifirst Enterprise
	TG-5005CE-21G	EPSON TOYOCOM	EPSON TOYOCOM
	1300269-16-16.368MHz	ITTI	ITTI
	KT3225F16368ACW28TA0	Kyocera	Kyocera
	ENG3090B	NDK	NDK
	7Q16300001-16.368MHz	TXC	TXC
TCXO (16.368 MHz) +/- 2.0ppm	TCO-5869M	EPSON TOYOCOM	EPSON TOYOCOM
TCXO 2520 (16.368 MHz)	IT2205BE 16.368 MHz	Rakon	Aurum Tech Inc.
	KT2520Y16368ACW28TMA	Kyocera	Kyocera

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Qualified Vender List -- LNA & LDO

Component	Part number	Manufacturer	Vendor
External LNA	NJG1117HA8	JRC	東鞍
	UPC8231	NEC	NEC
	MAX2659	MAXIM	MAXIM
LDO_2V8	XC6215/XC6401	Torex	敏茜
	AME8801CEEVZ	AME	AME
	TK71728	TOKO	華成

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Qualified Vender List --GPS Antenna

Circular-Polarized Patch	
Antenna Vendor	**Size (mm^3)**
Whayu	12X12X4, 13X13X4, 15X15X4
Yageo	12X12X4, 15X15X4
Mag.layers	15X15X4
CIRO	12X12X4, 13X13X4, 15X15X4
Amotech	13X13X4

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MT3326 HW Debug SOP

Verify voltage level of all power Supplies

↓

Check Connection of UART TXD & RXD

↓

Check GPS HW Configuration GPIO Setting & PMIC 2.8V

↓

GPS Function Ok!

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MTK GPS Phone Manufacture Flow

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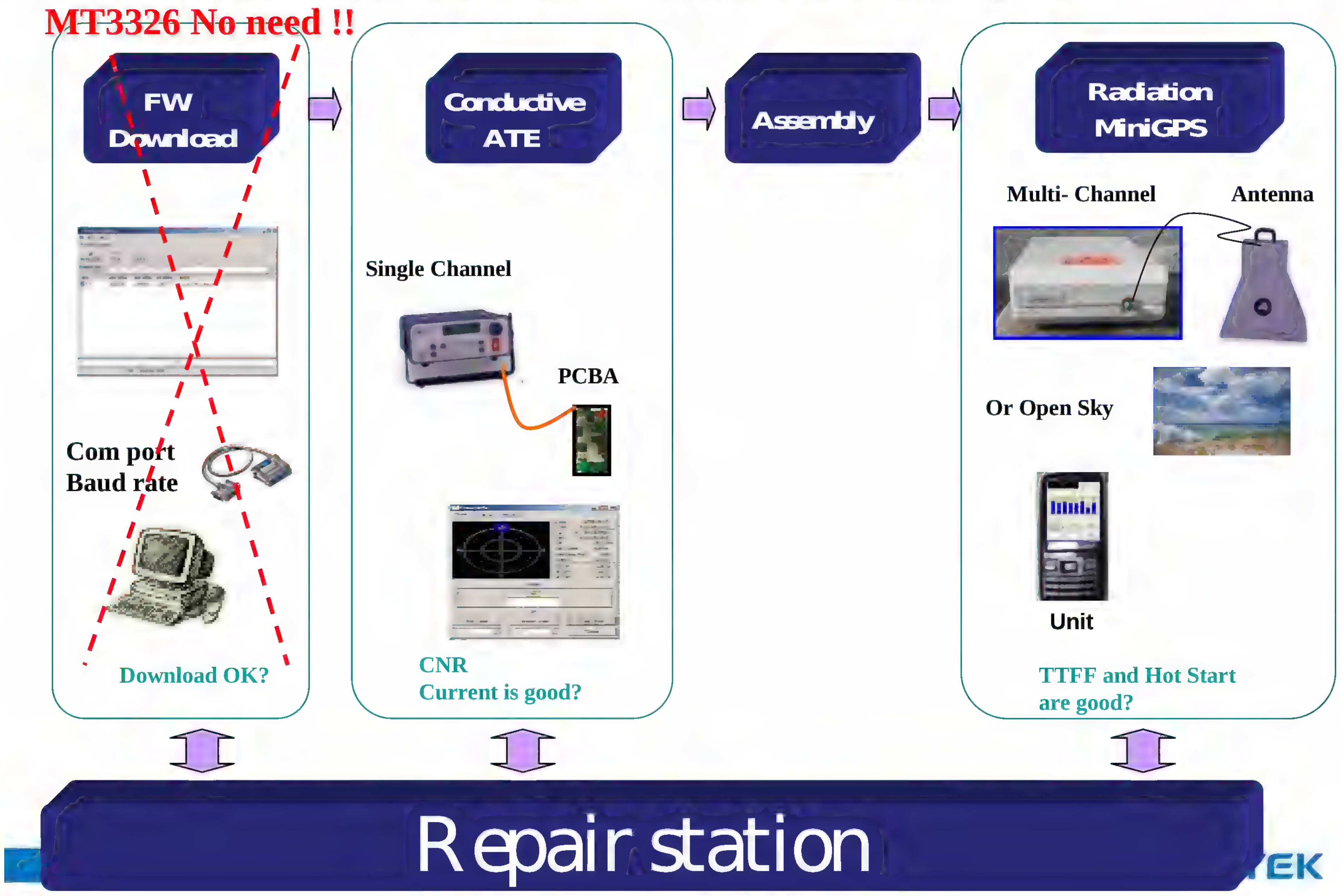
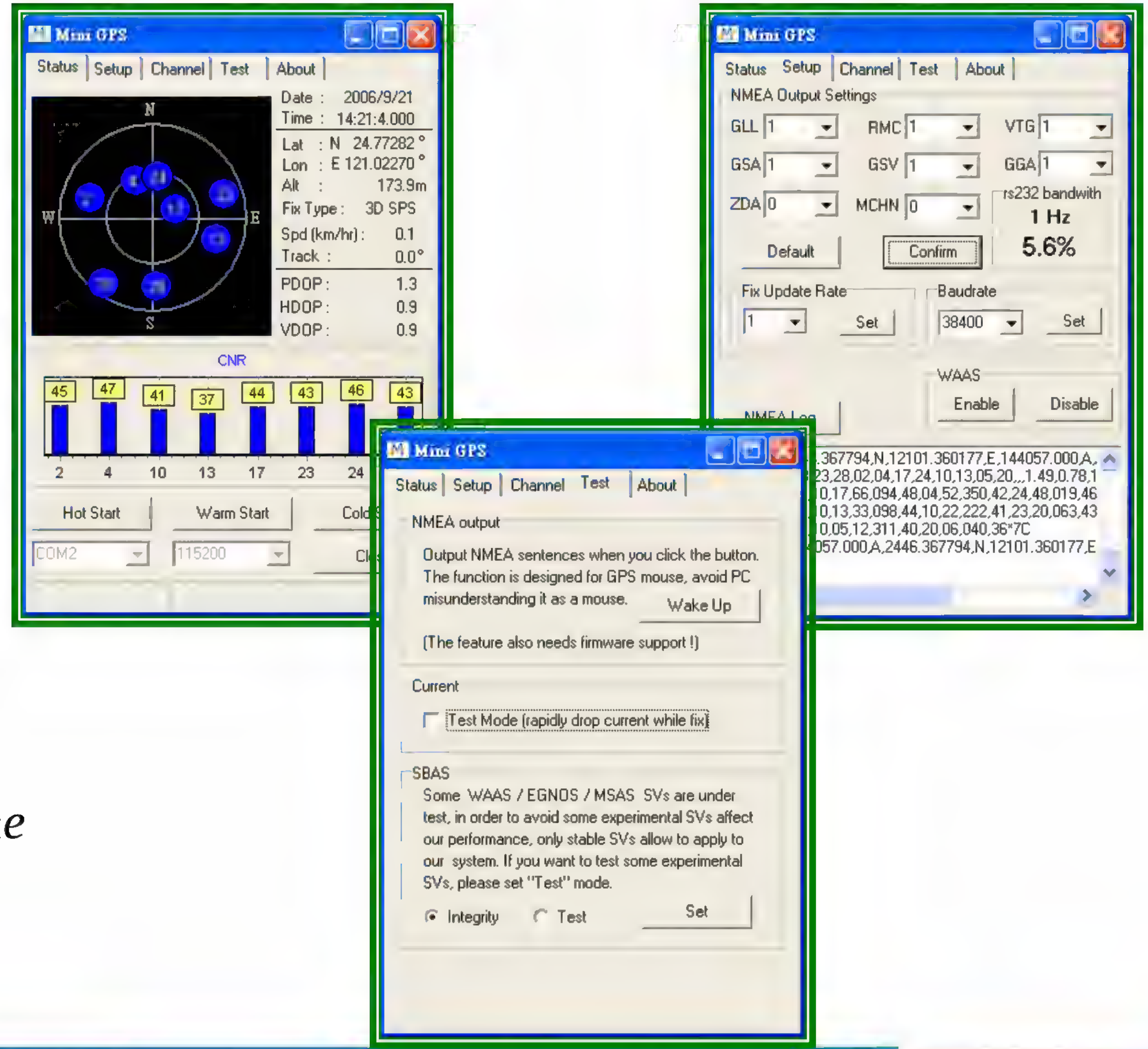


Mini GPS Tool (PC Version)

- *Feature*
  - *GPS Status*
  - *TTFF Test*
  - *NMEA Output*
  - *Update Rate*
  - *Baudrate*
  - *WAAS*
  - *Log NMEA*
  - *32 Channel*
  - *Firmware Ver.*

- *Usage*
  - *Customers*
  - *Production line*
  - *End users*



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Test Instruments (1/2)

Multi-Channel GPS Satellite Simulation System

Spirent GSS6560

Spirent STR4500

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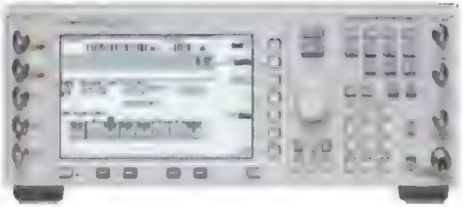
Test Instruments (2/2)

Areoflex

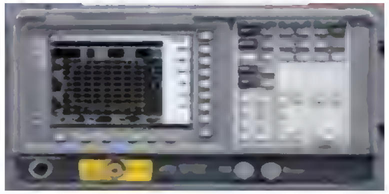
Single channel GPS-101 GPS Satellite Simulator

VNA

SA



SG



NFA

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DTV Application Note

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Outline

- **DTV function block and reference design**
  - DTV function block
  - DTV reference design

- **Reference interface assignment and key component**
  - Reference interface assignment
  - Key component

- **Schematic and layout design guide**
  - Schematic design guide
  - Layout design guide

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DTV Function Block and Reference Design

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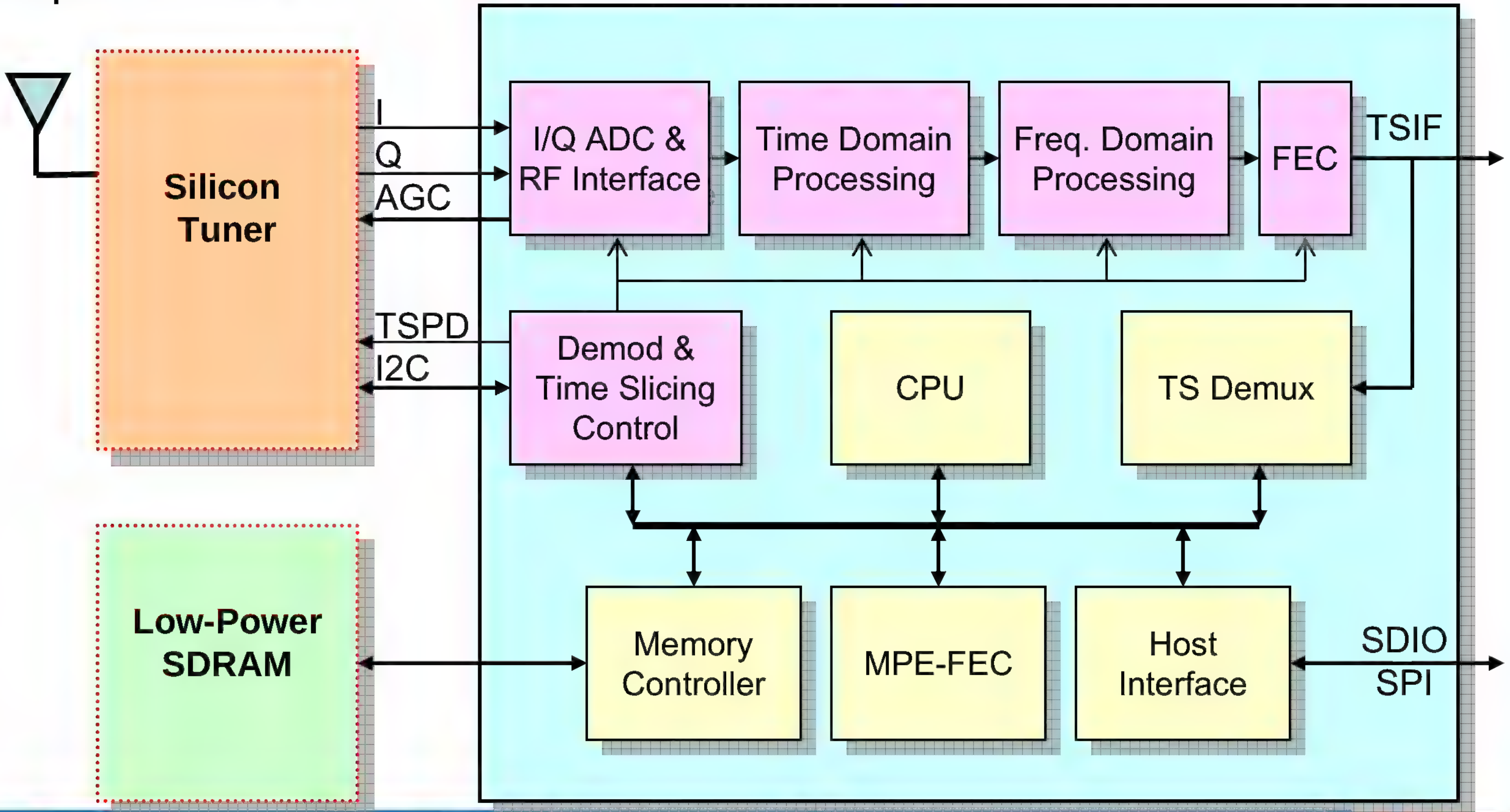
DTV Function Block

- DTV solution consists of MT5151, MT5162 tuner and one low-power SDRAM. It's integrated in MCM TFBGA-124 package to provide high integration level and high performance solution.
- MTK DTV solution provides worldwide DVBT compliant standard in VHF and UHF reception via the common SDIO/SPI interface.



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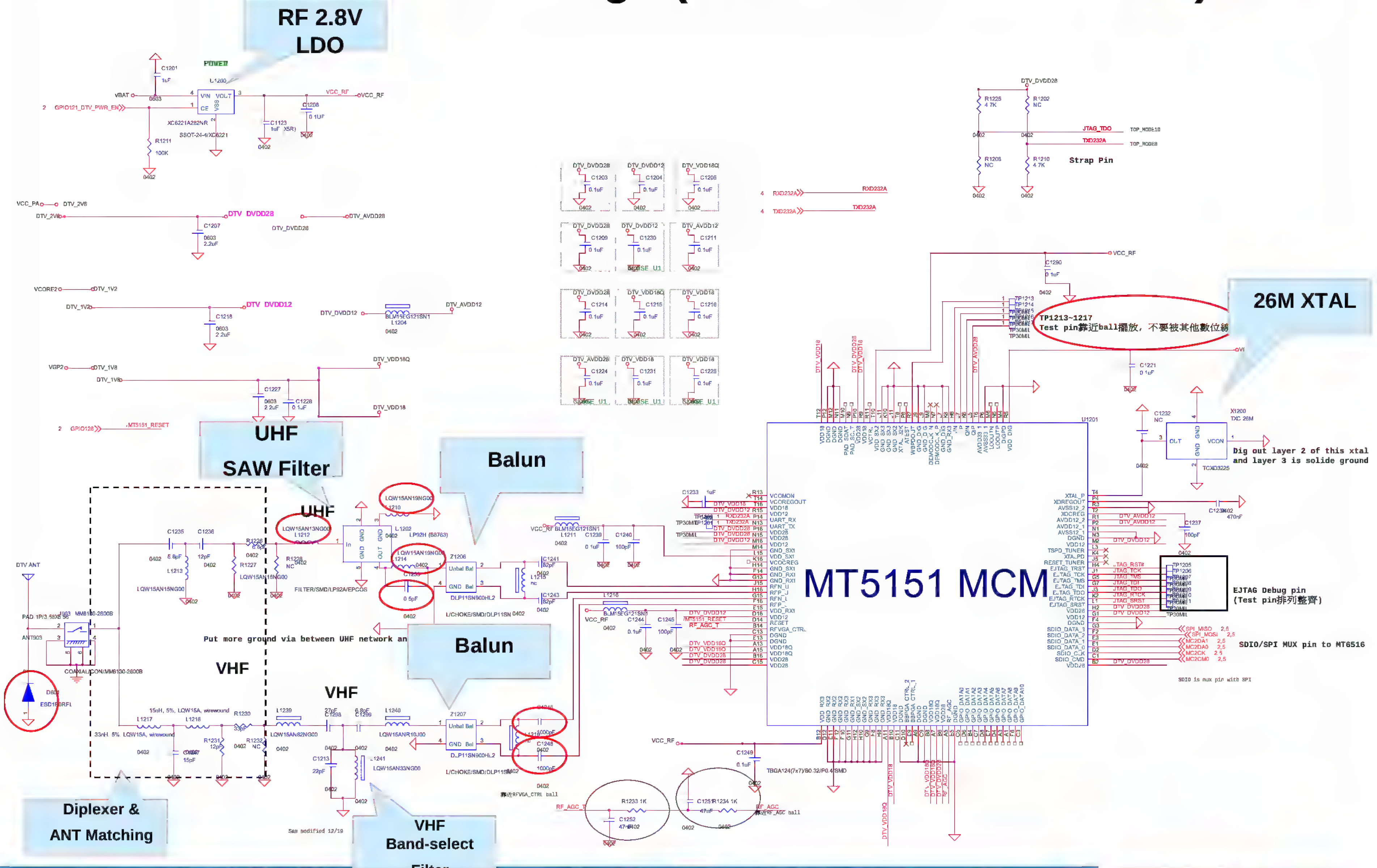
DTV Reference Design (Dual-Band: VHF & UHF)



DTV Reference Design (UHF band only)

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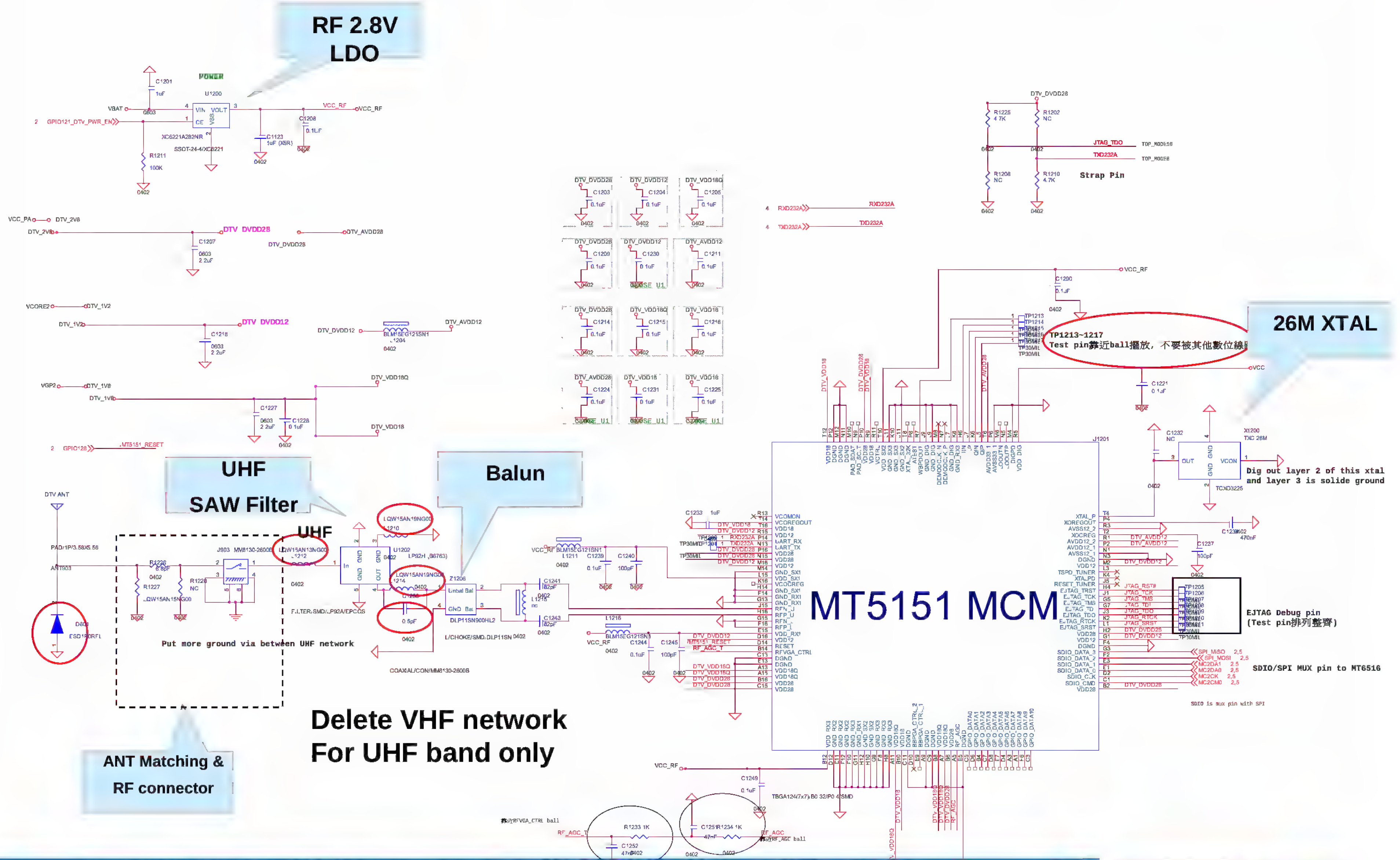

Delete VHF network
For UHF band only

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Reference Interface Assignment and Key Component

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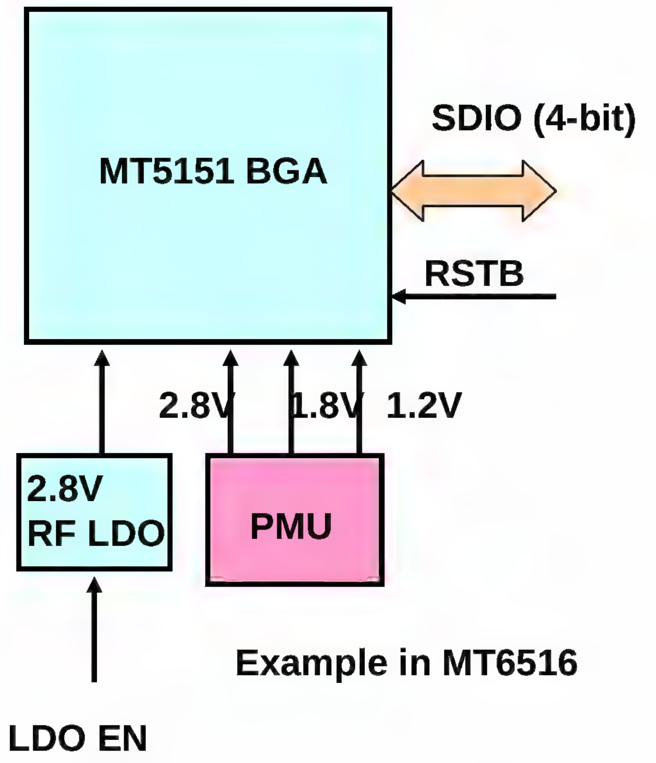
Reference Interface Assignment

Type	Pin	Function
GPIO	GPIO128	RSTB
	GPIO121	LDO EN
I/F	MC0CM0	SDIO
	MC0DA0	
	MC0DA1	
	MC0DA2	
	MC0DA3	
	MC0CK	



Example in MT6516

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Key Component

- There are four key components on DVBT reference design, SAW filter, crystal, Balun, and high Q wirewround inductor.

Item	Part number	Vendor	Designator
Filter	B8763 (LP92H)	EPCOS	U1202
Crystal	FL2600025	eCERA	X1200
Balun	DLP11SN900HL2	Murata	Z1206, Z1207
Inductor	LQW15A series	Murata	L1212,L1210,L1214,L1239,L1241,L1240 L1213,L1217,L1218

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Schematic and Layout Design Guide

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Schematic Design Guide

- The ESD protection of RF input is poor, ESD device should be added to protect RF circuit.
- UHF SAW filter & VHF hybrid filter should be added in RF path to filter out-band and GSM interference signal.
- To ensure good performance, the frequency accuracy of crystal should meet +/- 30 ppm requirement with loading capacitance SPEC of 10pF.
- In order to have better power noise immunity, RF 2.8V supply voltage is provided by stand-alone LDO.
- IO-2.8V and SDRAM-1.8V should be provided by linear regulation power. Core-1.2V could be DC-DC power.
- RF Balun is strongly suggested to use for optimal RF performance

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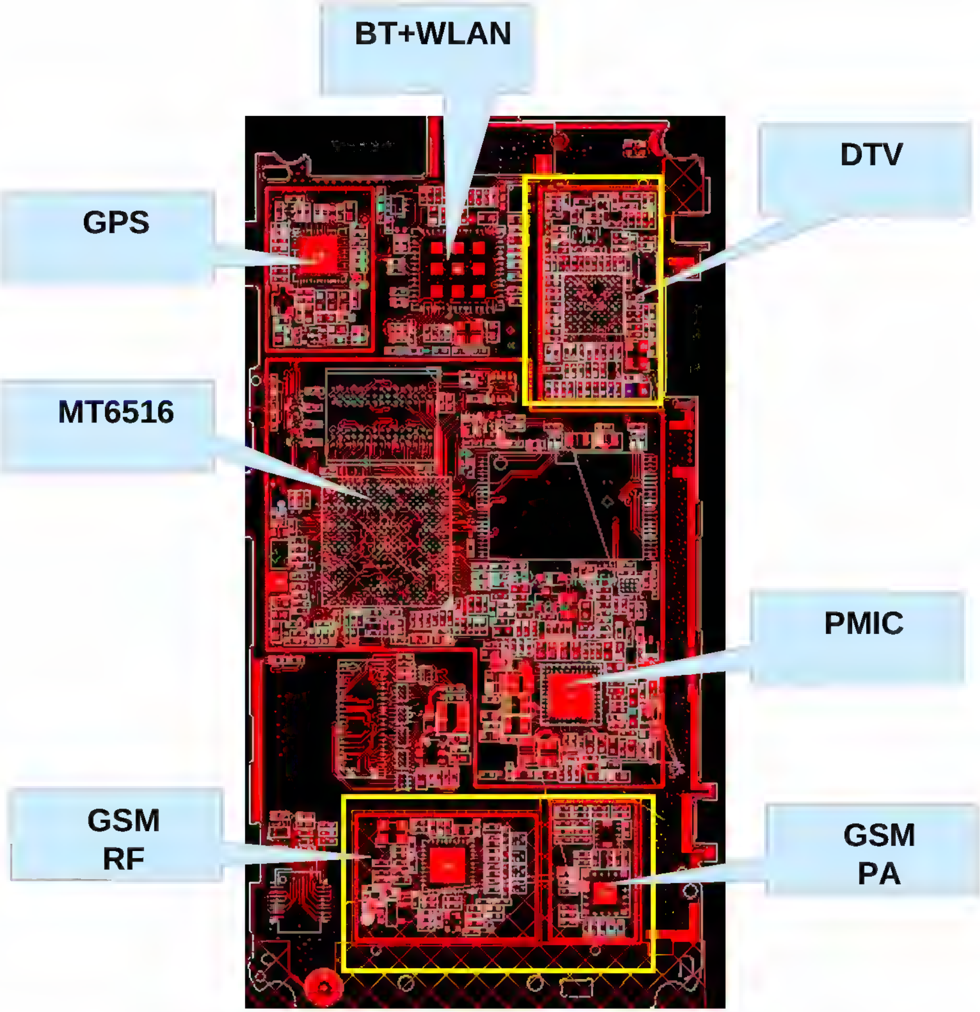
DTV Layout Guide – 1/3

- DTV placement should keep away from GSM and CDMA related circuits.
- Don't place DTV near noisy components, such as PMIC, memory or other clock-wise/ high-swing signal.
- RF trace of DTV should keep away from high speed signal, such as LCD and camera data bus.
- To avoid any other noisy layout closer to RF ANT port
- Put solid ground polygon and ground via surround layout area for metal casing.



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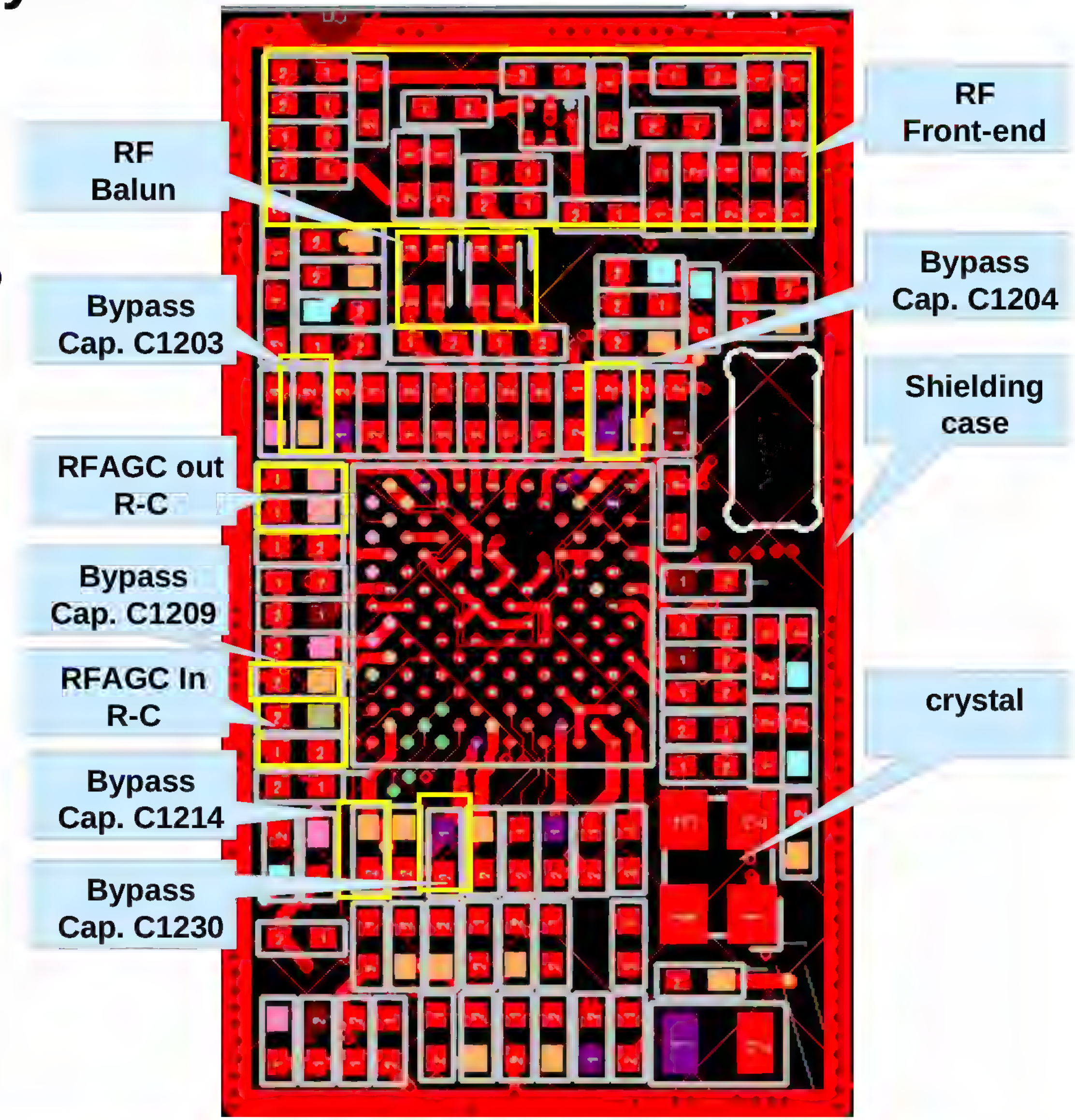
DTV Layout Guide – 2/3

- Keep RF trace on same layer, don't use via on RF trace as possible as you can.
- To avoid interference, use shielding case to cover DTV related circuits.
- Put RF Balun as closer as possible to chip input. And Make routing symmetrically.
- Put RF front-end routing in 50ohm trace and let those inductors in orthogonal direction with each others.
- Place 2.8V RF LDO and crystal near to MT5151 as possible as you can.
- Dig out the copper plating under Crystal pad output (pin3) to chip in inner layer .
- RF trace should keep 50ohm impedance and as short as possible.
- Place bypass capacitors close to power pin.
- Put DTV's off-chip components surround by it in sequence to minimize rounting.
- Put RFAGC in/ out R-C network as closer as possible to pin



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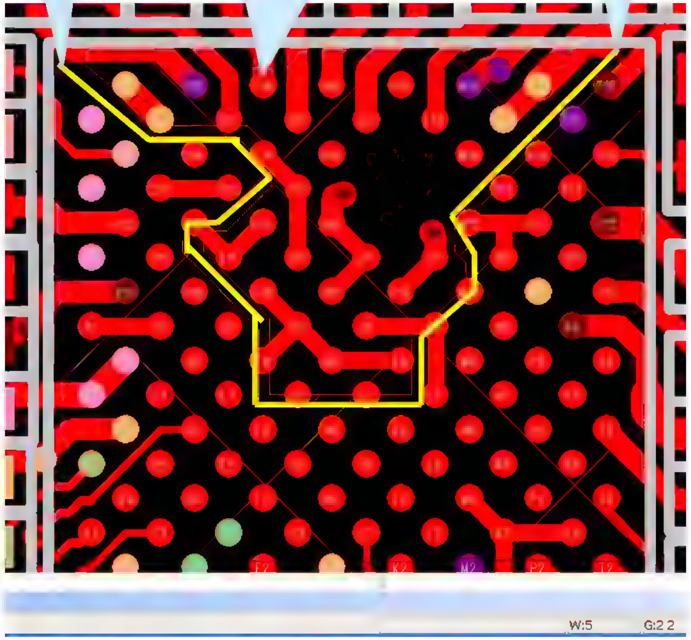
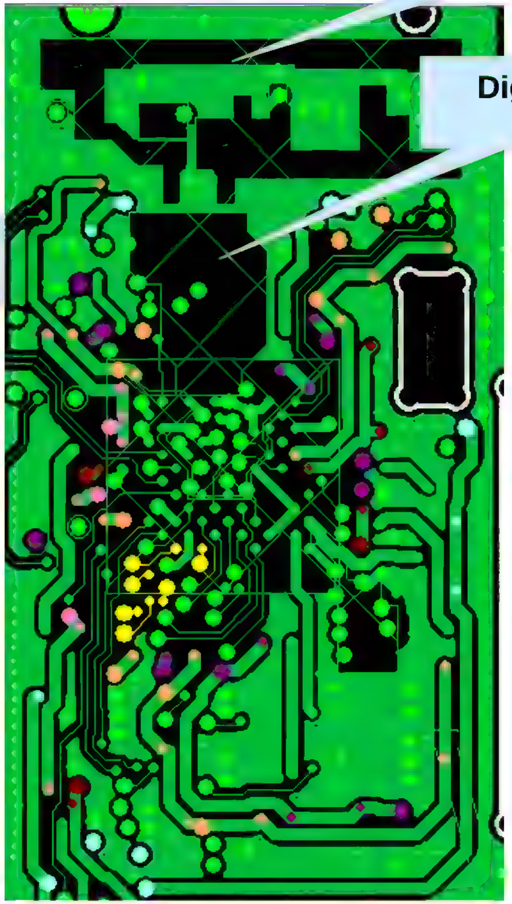
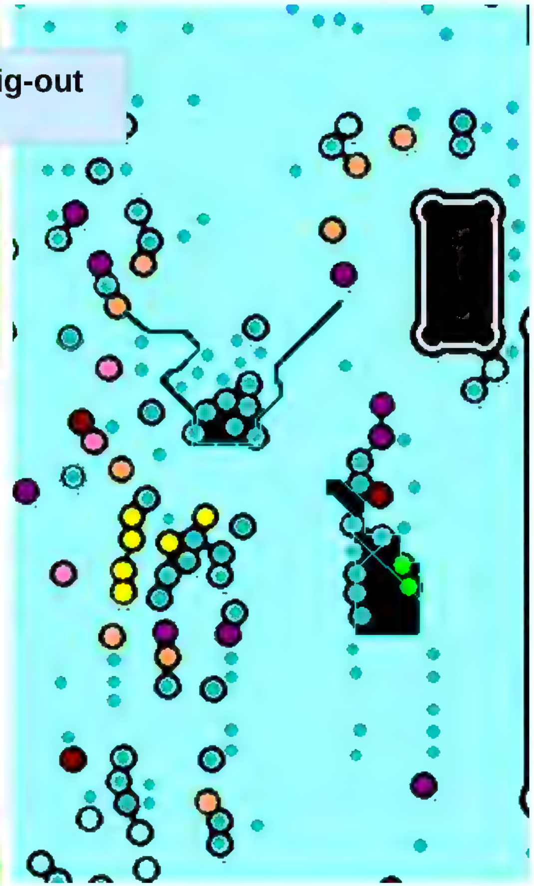
DTV Layout Guide – 3/3

- As below shown, make a dig-out clearance gap (>= 6mil) to cut ground plane from layer 2 to layer 6 to isolate RF and digital GND.
- Dig out layer 2 ploygon under RF front-end network







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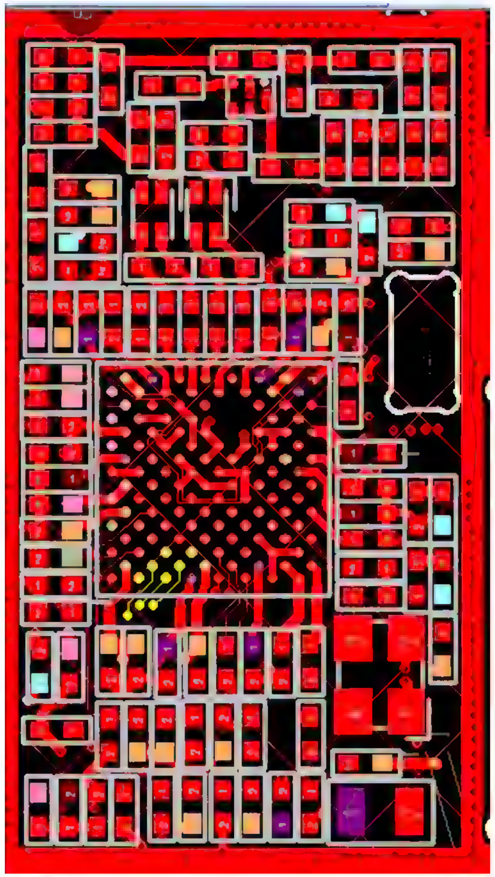
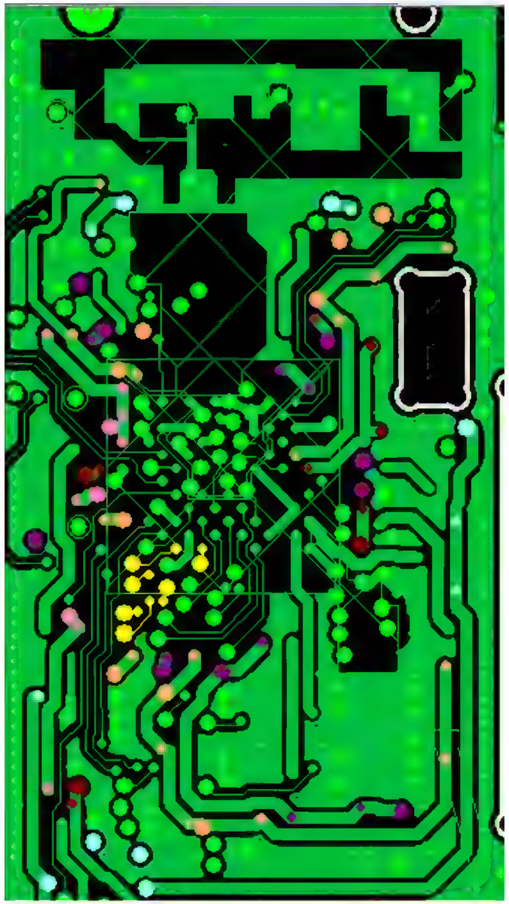
Reference Layout – 1/4

Layer1



Layer2



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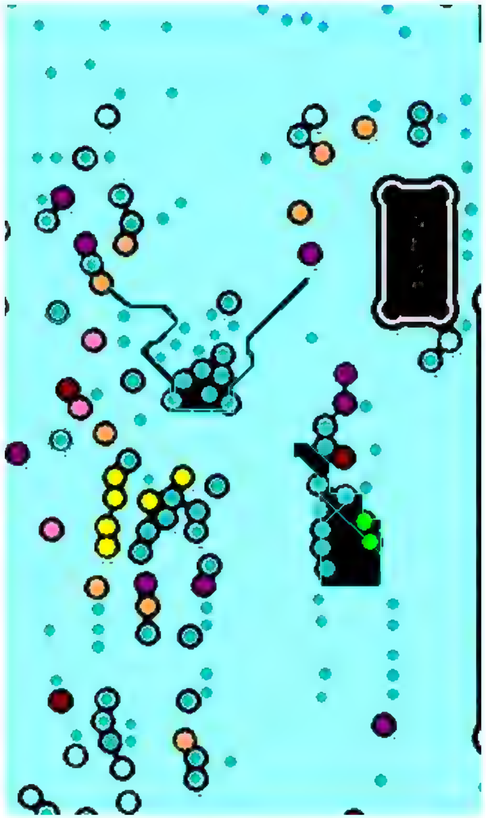
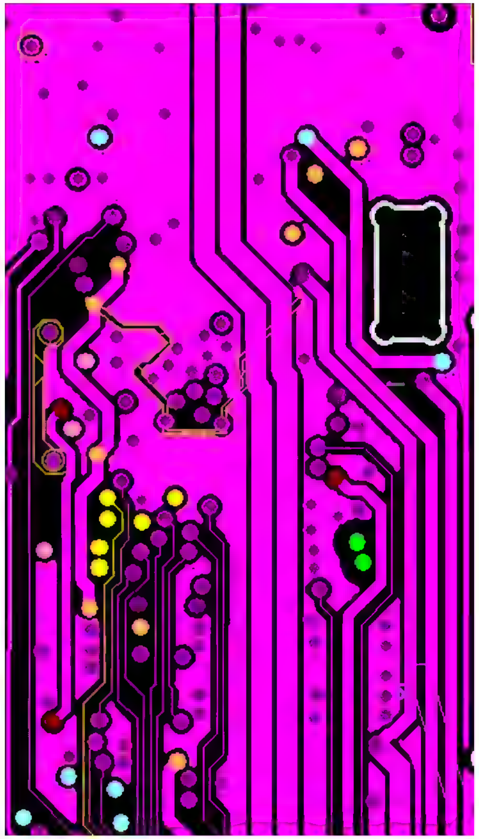
Reference Layout – 2/4

Layer3



Layer4



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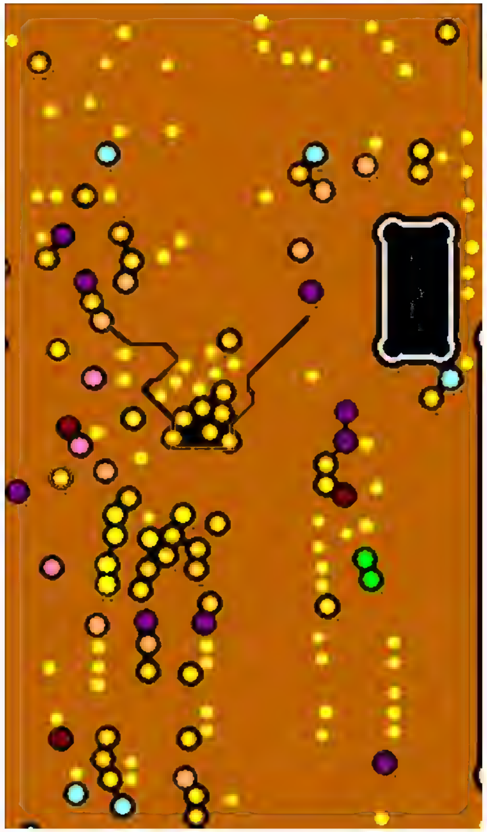
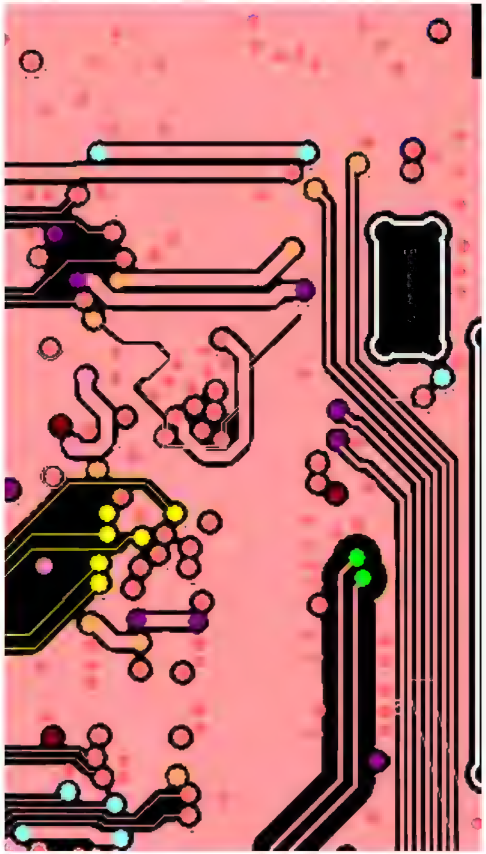
Reference Layout – 3/4

Layer5



Layer6



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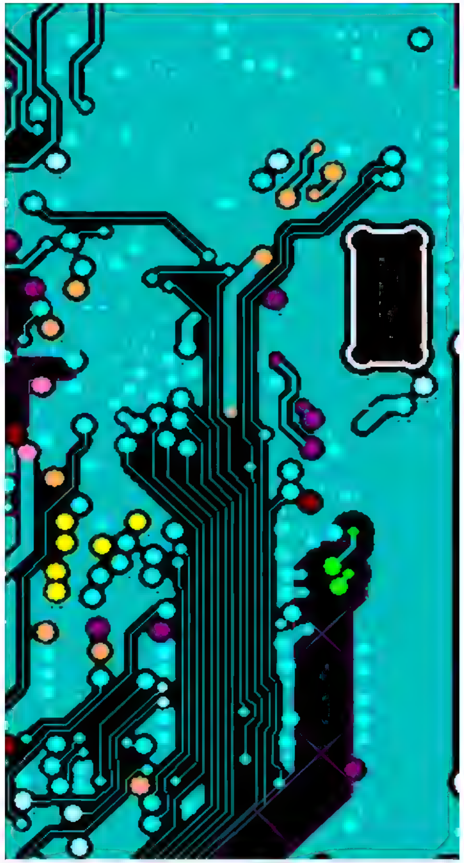
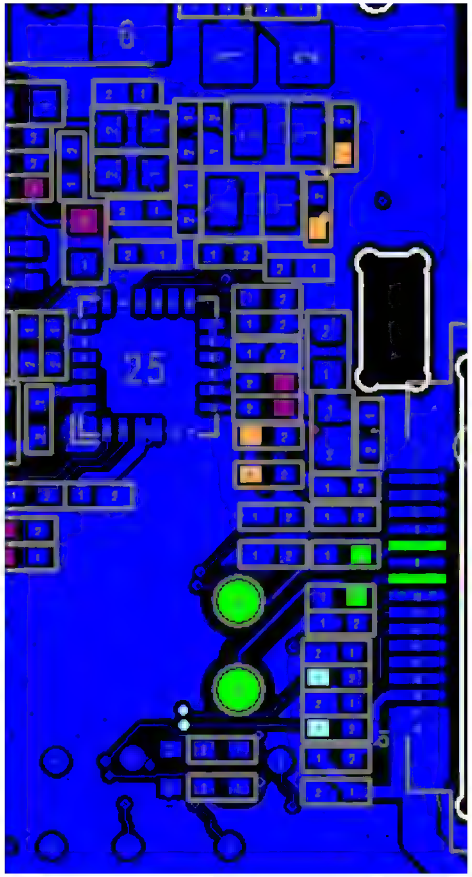
Reference Layout – 4/4

Layer7



Layer8



(other function placement instead of DTV)

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FM Radio Design Guidelines

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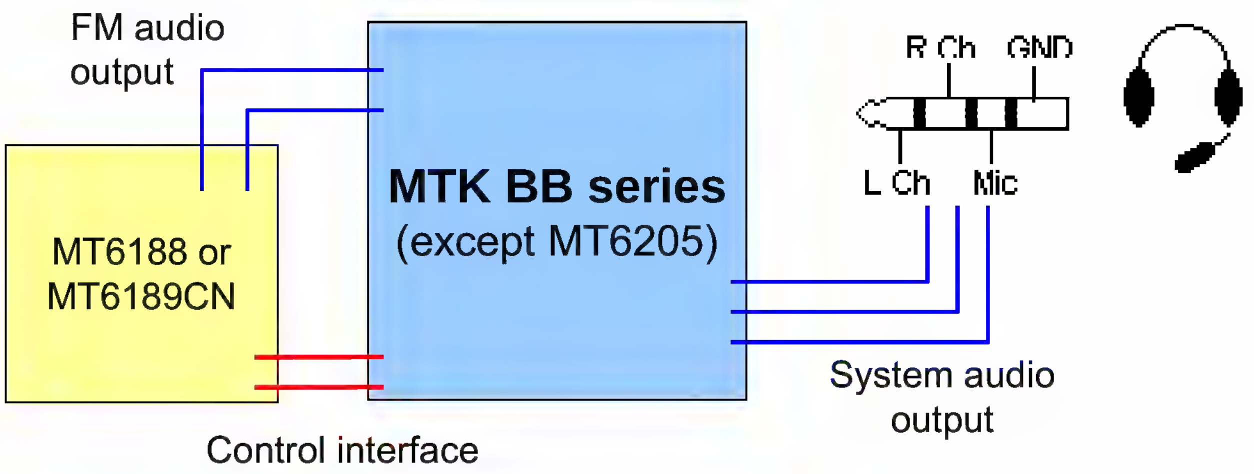
MTK FM Solution Connection



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FM Design

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Layout Guidelines

- **Placement**
  - Place the FM chip near the earphone jack. **Avoid high-speed digital devices, such as memory devices, near the RF signal area.**
  - Bypass cap for power should be placed beside the VCCVCO pin (MT6188 pin 9; MT6189 pin 13).
- **Routing**
  - FM antenna trace should have a 50Ω impedance.
  - Power should be routed to the bypass cap and the VCCVCO pin first, then to all other power pins on the FM chip. See the following pages for example.
  - Apply a single solid ground for all FM block ground signals. See the following pages for example.
  - Protect the following areas with GND vias and planes:
    - RF signal from the earphone jack all the way to the FM chip;
    - 32.768 kHz or 26 MHz signal;
    - VCO inductor (MT6188 pins 11,12; MT6189 pins 15,16);
    - Loop filter of MT6189 (connected to pin 17).

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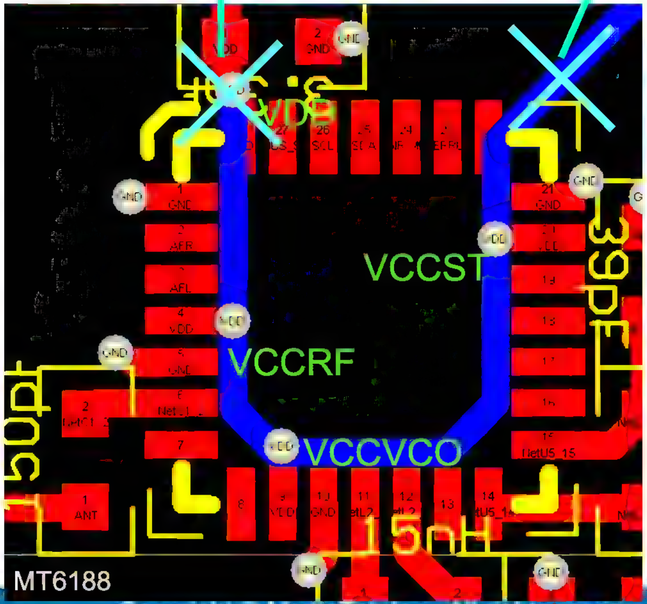
Power Feeding Network Layout Guidelines

- It is recommended to connect power of MT6189 and MT6188 sequentially, and placing the capacitance beside VCCVCO. (Examples below.)
- The FM power should be monopolized: do not connect other blocks to VCC_FM.

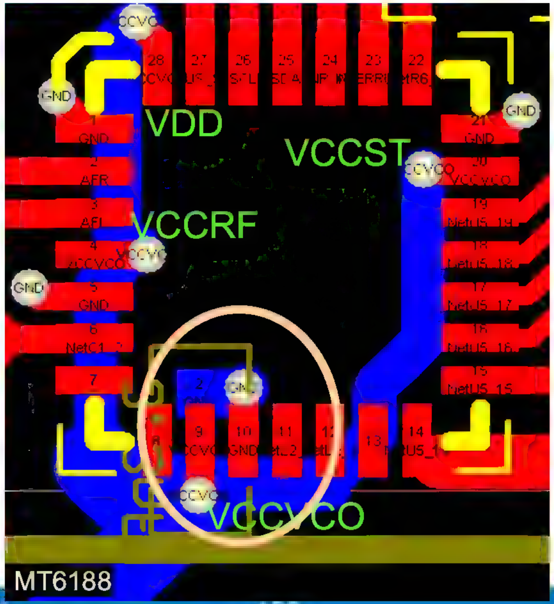
This capacitor cannot be placed here.

Do not connect to other blocks through FM block.

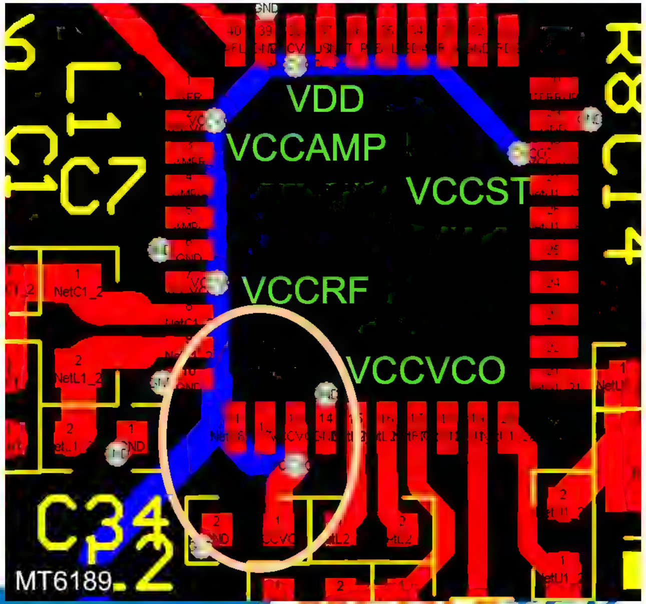
Bad



Good



Good



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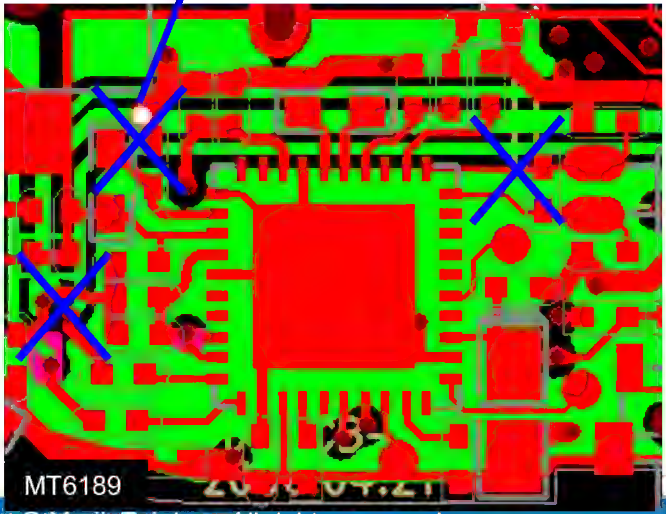
Ground Layout

- Ground GNDVCO, the loop filter, and front-end matching on the same ground plane.
  - Using different ground planes connected by wire makes the FM signal susceptible to interference with another signals on the system.
  - This rule is applicable for both MT6189 and MT6188: all GND pins must be located on the same ground plane.

All ground pins are connected by wires.
This design contains no ground plane.

Bad



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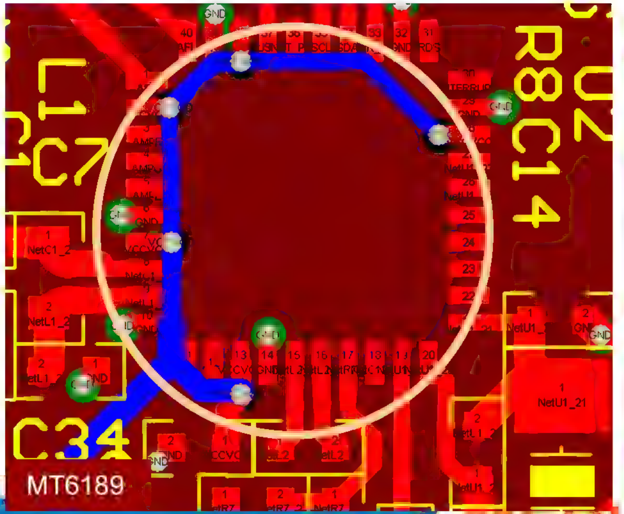

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Other System Considerations for FM

- **Rule 1: Protect the BB 32.768kHz crystal layout**
  - If the 32.768kHz signal is corrupted by digital signals, FM channel locking may be unstable.
  - BB 32.768kHz crystal layout rules:
    - Place the 32.768kHz crystal unit close to the BB, and L2 beneath crystal needs to be complete ground. The crystal must be protected by ground vias and ground planes.
    - Do not route power, MCP, FM I2C traces near 32.768kHz crystal unit.
    - The 32.768kHz traces between crystal unit and BB should be on top layer.
- **Rule 2: Backlight driver adoption**
  - USE a charge pump backlight driver.
  - DO NOT USE a DC-DC backlight driver in projects with FM application. Doing so may cause increased noise levels when the backlight is on.

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Audio Interface Design

- *2.5mm/3.5mm Earphone*
- *Mini USB Earphone*

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Audio Interface Design Guidelines

- On earphone pins AFL, AFR, and MIC:
  - Place **1 nF** shunt capacitors (shunt to earphone GND pin) closest to the earphone jack.
    To improve earphone echo performance, connect the 3 capacitors from each pin to the earphone GND pin separately. (See next page.)
  - Place the **BLM18BD252SN1** series bead second closest to the earphone jack.
  - No other components can be closer to the earphone jack.
- Place a series **150 nH** inductor on earphone GND pin as antenna matching.
- Earphone GND wire (FM_ANT) should not be connected to the earphone connector shell.
- An earphone **longer than 150 cm** is recommended for better performance.

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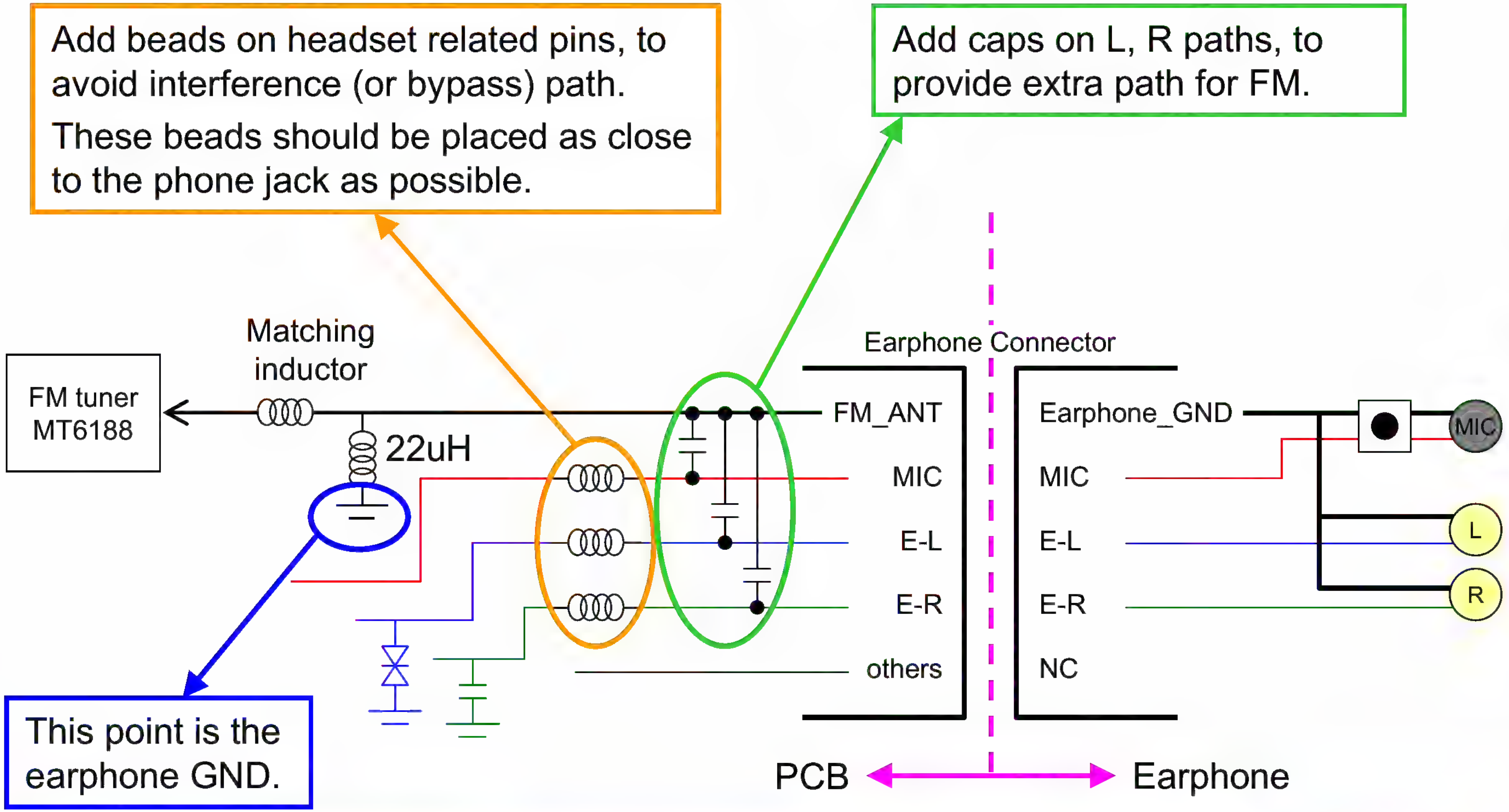
Audio Interface Design Concept



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Wireless Sensitivity Enhancement

- Each earphone suggestions improves wireless sensitivity significantly. The following table shows the improvement amount based on MTK's experiments.

	Improvement amount
Series beads on earphone AFL, AFR, and MIC pins	14.5 dB
1 nF shunt cap between earphone AFL, AFR, MIC, and GND pins	2~3 dB
Earphone length > 150 cm	1~2 dB

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2.5mm/3.5mm Earphone Design

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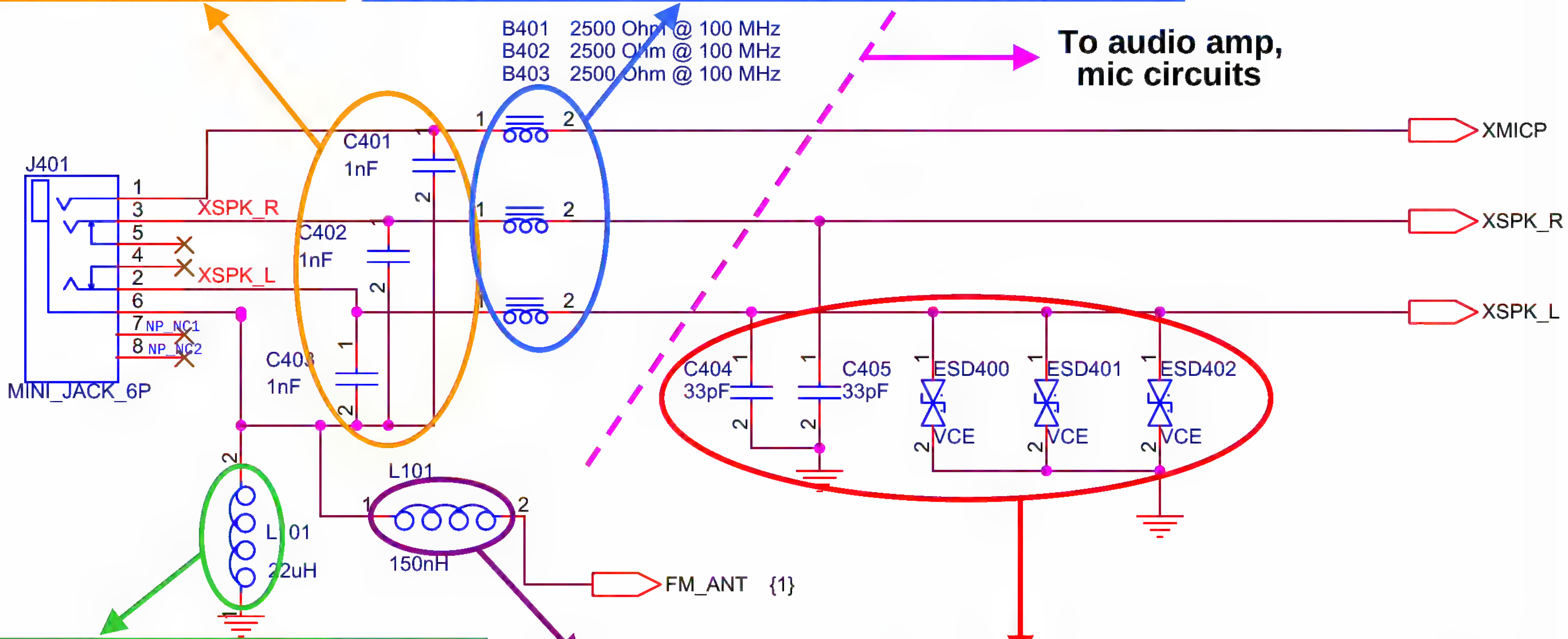
Audio Interface Reference Circuit
(2.5mm or 3.5mm Earphone Jack)

Shunt these earphone lines with 1nF caps.

Add beads on these lines. **These beads should be placed as close to the earphone jack as possible.**



Connect this 22uH inductor to mobile phone ground. **BLM18BD252SN1** can be used instead of a 22 uH inductor.

Series 150 nH inductor for antenna matching.

These caps cannot be closer to the earphone jack than the beads.

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Mini USB Earphone Design

- With only 1 GND pin on IO connector
- With 2 GND pins on IO connector

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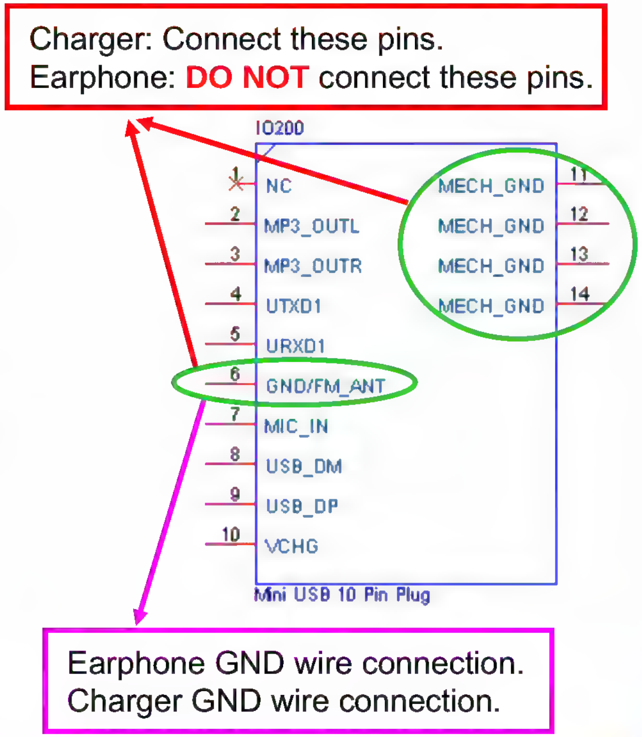
Mini USB IO Connector Design Recommendation: Only 1 GND Pin on IO Connector

Accessory interior design suggestion

- The earphone GND wire MUST be used for the FM antenna. Inside the earphone, the GND wire CANNOT be connected to any other wire or to the outer shell in any way. Other wires inside the earphone CANNOT be connected to PCB GND.
- The 22uH inductor cannot tolerate high current. For high current application, such as a charger, connect the charger GND wire inside the charger to both the GND/FM_ANT pin and the charger outer shell.
- In this example, the earphone GND wire is connected to IO connector pin6, and the charger GND wire is connected to pin6 and the charger outer shell.



IO connector pin description

IO pin name	Function	Notes for PCB design
GND/FM ANT	GND for all Mini USB accessories and FM antenna.	CANNOT be directly connected to PCB ground. MUST be connected to PCB ground through a 22uH inductor.
MECH_GND	4 outer shell pins of the IO connector. Mainly used for better connector strength. Can also serve as charger GND.	These 4 pins are directly connected to PCB ground. DO NOT connect these pins to the GND/FM_ANT pin.

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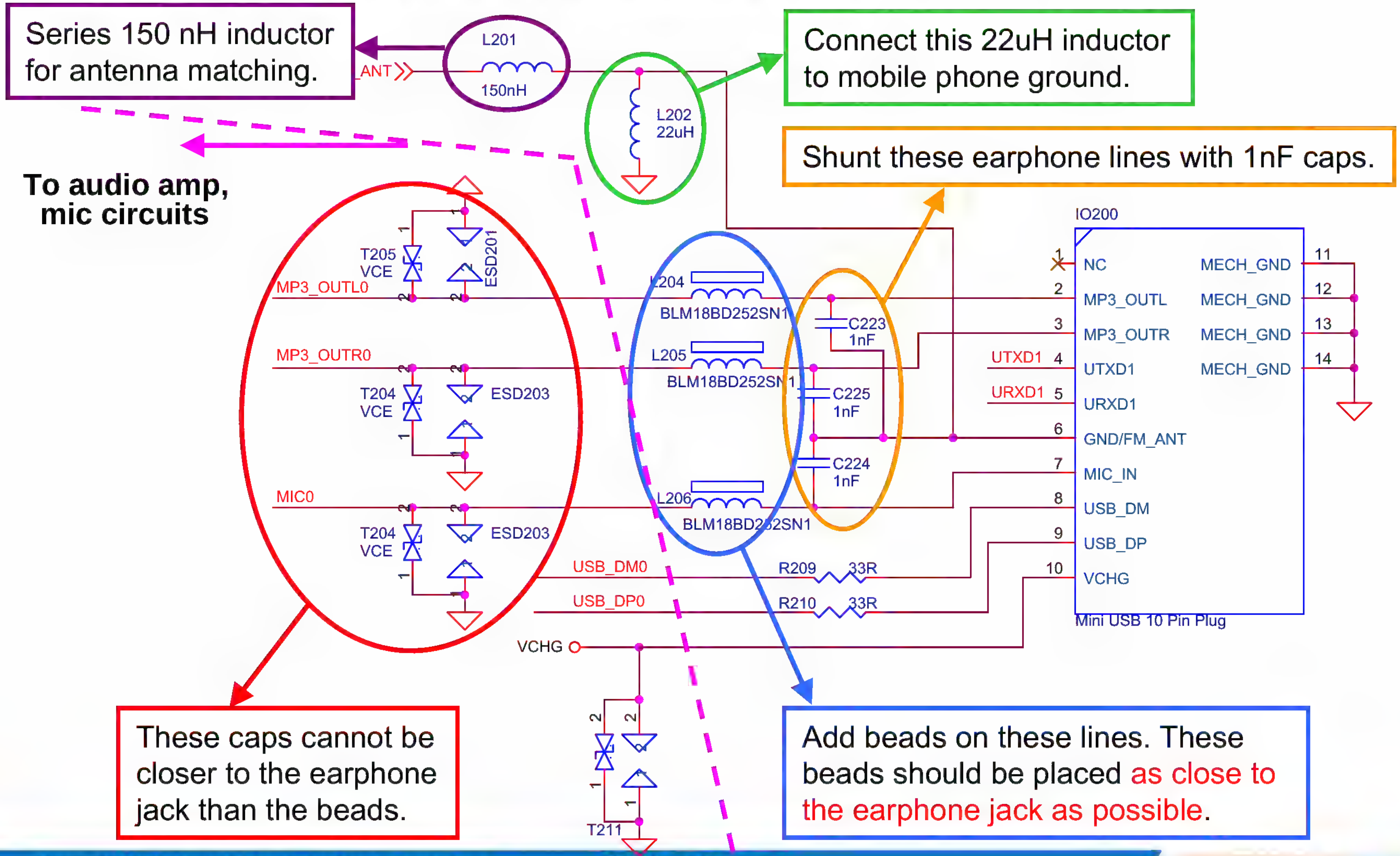
Audio Interface Reference Circuit:
Only 1 GND Pin on IO Connector



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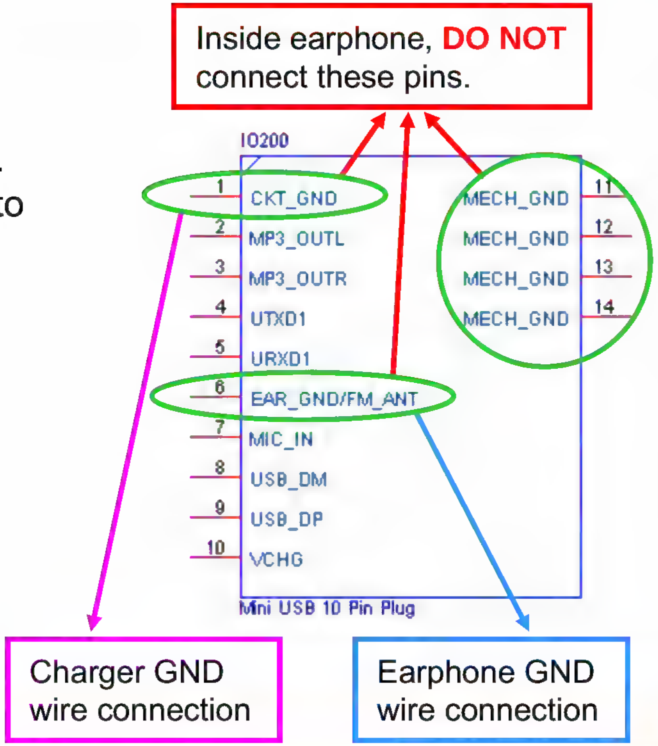
Mini USB IO Connector Design Recommendation: 2 GND Pins on IO Connector

Accessory interior design suggestion

- The earphone GND wire MUST be used for the FM antenna. Inside the earphone, the GND wire CANNOT be connected to any other wire or to the outer shell in any way. Other wires inside the earphone CANNOT be connected to PCB GND.
- The 22uH inductor cannot tolerate high current. For high current applications, such as a charger, use another IO connector pin if available. The charger GND wire inside the charger can also be connected to the charger outer shell.
- In this example, the earphone GND wire is connected to IO connector pin6, and the charger GND wire is connected to pin1 and possibly the charger outer shell as well.



IO connector pin description

IO pin name	Function	Note for PCB design
EAR_GND/FM_ANT	Earphone GND, also FM antenna.	CANNOT be directly connected to PCB ground. MUST be connected to PCB ground through a 22uH inductor.
CKT_GND	GND for Mini USB accessory, with large GND current.	This pin is directly connected to PCB ground. DO NOT connect this pin to the EAR_GND/FM_ANT pin.
MECH_GND	4 outer shell pins of the IO connector. Mainly used for better connector strength. Can also be served as charger GND.	These 4 pins are directly connected to PCB ground. DO NOT connect these pins to EAR_GND/FM_ANT.

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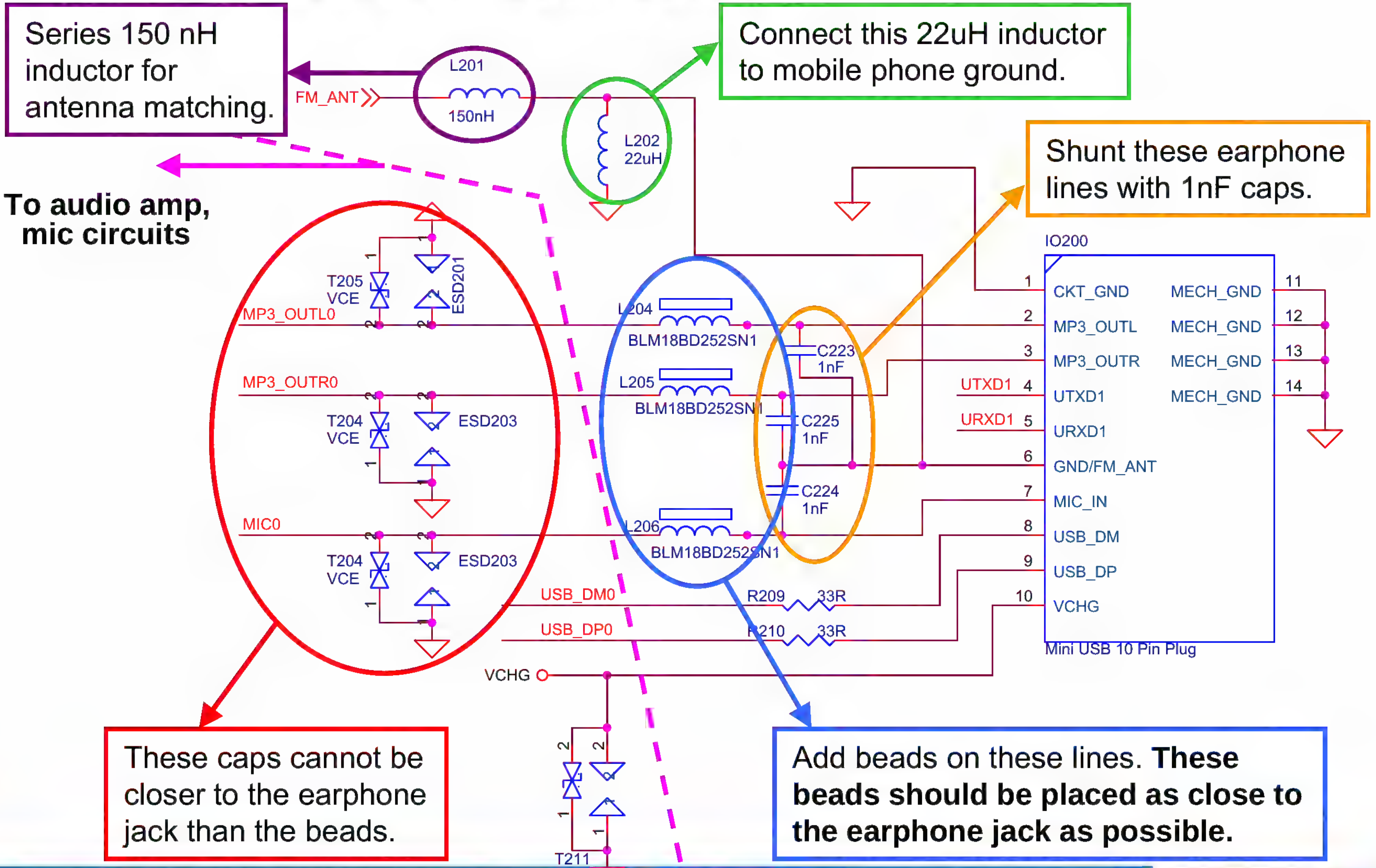
Audio Interface Reference Circuit:
2 GND Pins on IO Connector



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Component Replacement Suggestions

- Series beads on earphone pins AFL, AFR, and MIC
  - Suggested: 0603-size BLM18BD252SN1 bead
    However, if board space is limited, 0402-size bead BLM15BD182SN1 or BLM15HD182SN1 can be used instead.
- Inductor connecting earphone GND wire to board GND
  - Suggested: 22 uH inductor or BLM18BD252SN1 bead
    However, if the earphone GND pin serves as the only GND path for the charger, then this component must be able to tolerate high current. The components in the table below can be used instead.

Murata part number	Inductor value	Size	Self-resonant frequency	Rated current	Notes
LQH2MCN1R0M02	1.0 uH	0603	100 MHz	485 mA	
LQM21PN1R0MC0D	1.0 uH	0805	90 MHz	800 mA	
LQM21PNR47MC0D	0.47 uH	0805	100 MHz	1100 mA	Usable, but its wireless performance is the worst among the three. Not recommended unless such a high current is required.

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FM Design Checklist

Item	Done!	Checkpoint
1	☐	Series beads are placed on the AFL, AFR, and MIC pins of the earphone jack.
2	☐	1 nF shunt caps are placed between the AFL, AFR, MIC, and GND pins of the earphone jack.
3	☐	The earphone is longer than 150 cm.
4	☐	The VCC bypass cap is placed beside the VCCVCO pin, and the VCC feeding network routed is properly.
5	☐	Follow the FM system layout guide.
6	☐	The FM antenna path is routed using a 50Ω RF trace, and a 150 nH inductor is used for antenna matching.
7	☐	***MT6189 projects only***: A high Q inductor is used (for the 15 nH VCO inductor).
8	☐	***Mini USB earphones***: Follow MTK's suggestion for GND connection on PCB and inside earphone.

If you require MTK's assistance in FM design, please prepare this checklist and submit it along with schematics, layout files and earphone schematics/data sheet.

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More Detailed FM Earphone Antenna Illustrations

- *Illustration of FM earphone antenna*
- *FM earphone antenna pin definition*
- *FM earphone antenna troubleshooting*

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Illustration of FM Earphone Antenna (1/2)

- On next page, there is an illustration to explain the respective purposes of each components. It can help customers to know how to enhance FM wireless performance.
- Besides FM schematics, wrong earphone pin definition also destroys FM wireless performance.
- Notice that the only one path from Earphone_GND to PCB_GND is via FM_ANT Pin and 22uH. If there are another paths existing, FM receiving signal would degrade seriously. **This issues frequently happens on customers' projects.**
- Four pins are enough on earphone including R, L, MIC, and Earphone_GND.
- Only Earphone_GND can be used as FM Antenna.
- Place all FM related components near earphone jack in PCB layout.

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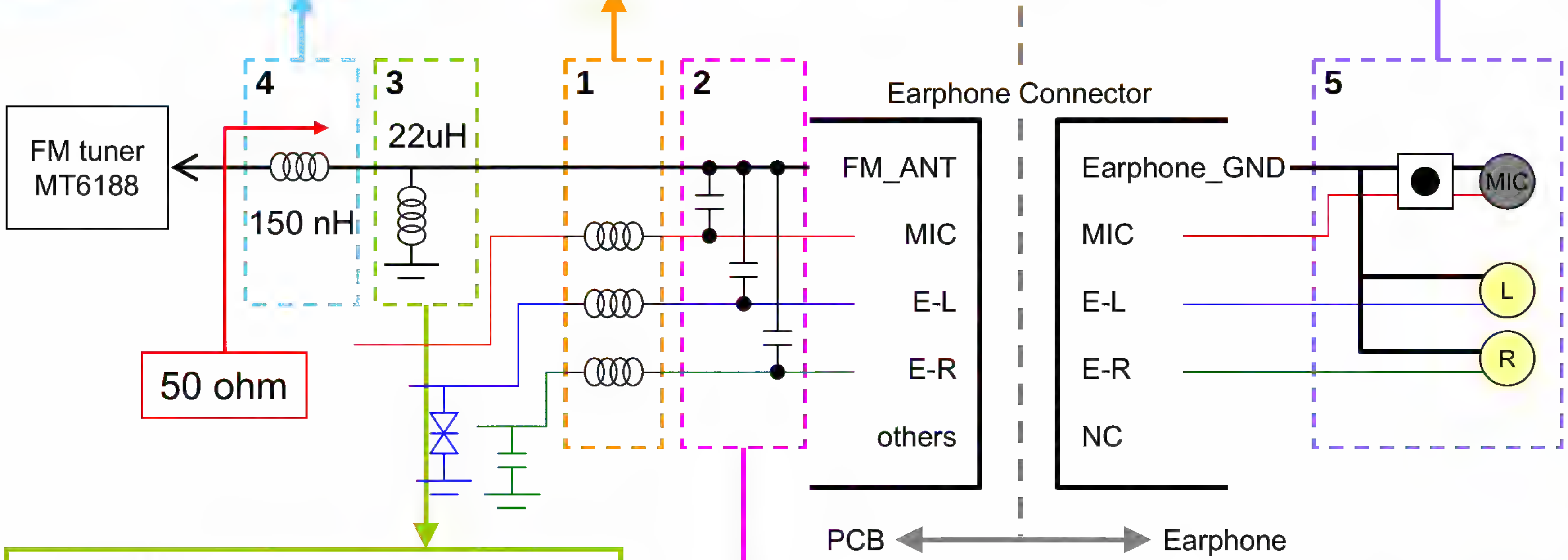
Illustration of FM Earphone Antenna (2/2)

4. 150 nH
   Earphone antenna matching

1. Serial Beads 2.5 kOhm @100MHz
   Avoid FM signal loss through R, L, and MIC traces.

5. Earphone length
   165 cm is recommended.



3. 22 uH
   - Earphone GND connects to PCB GND only via this 22 uH.
   - RF choke @100MHz

2. Parallel 1.0 nF CAP_short @100MHz
   Conduct FM signal to FM input from R, L, and MIC traces. FM receiving signal can be enhanced.

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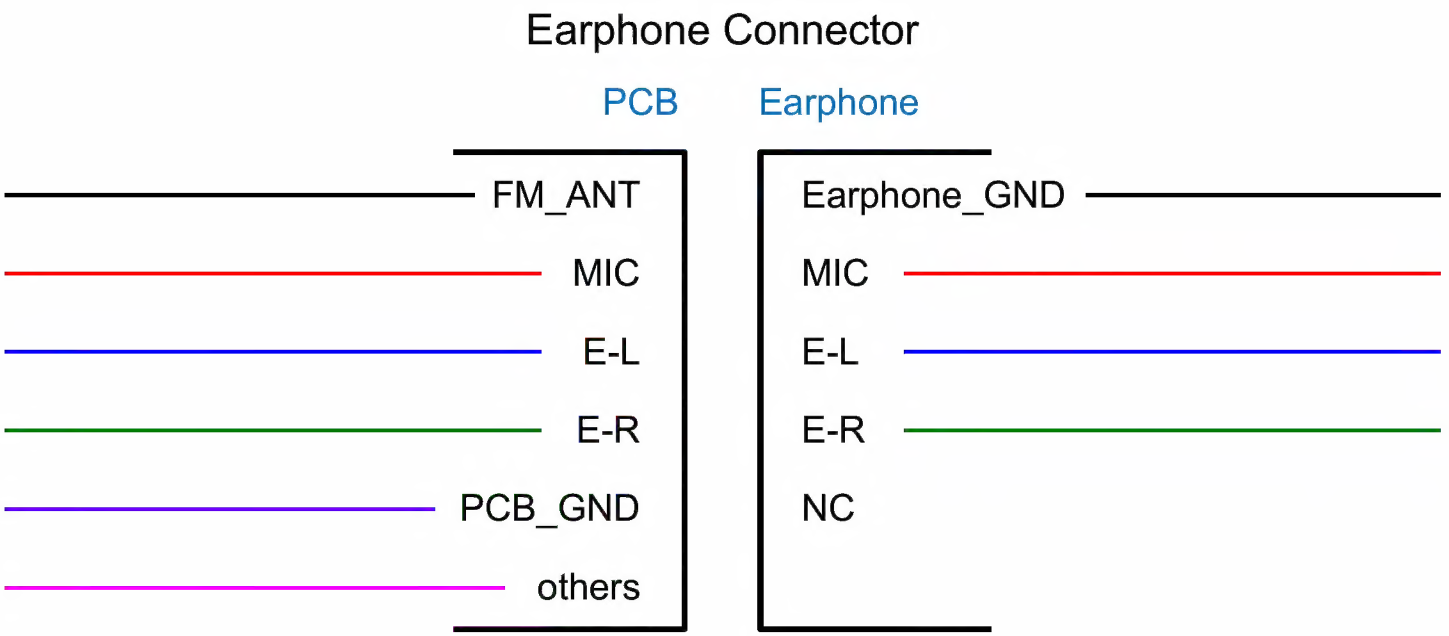
FM Earphone Antenna Pin Definition (1/3)

- The following illustrates the correct pin definition for the FM earphone antenna:



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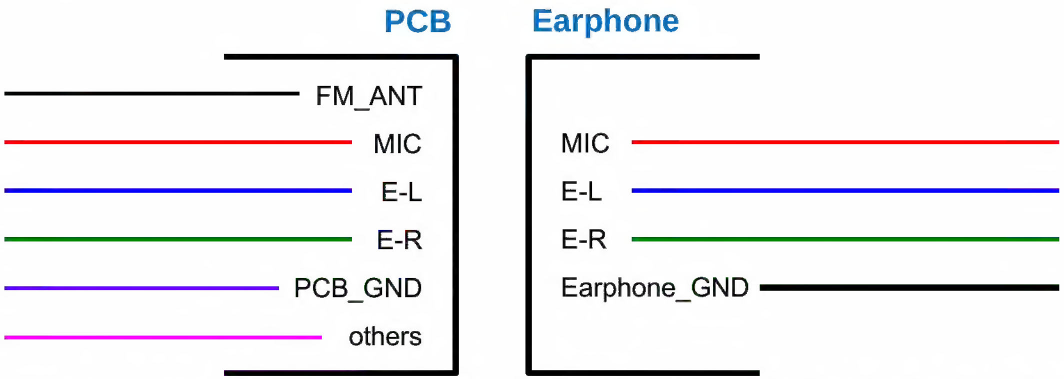
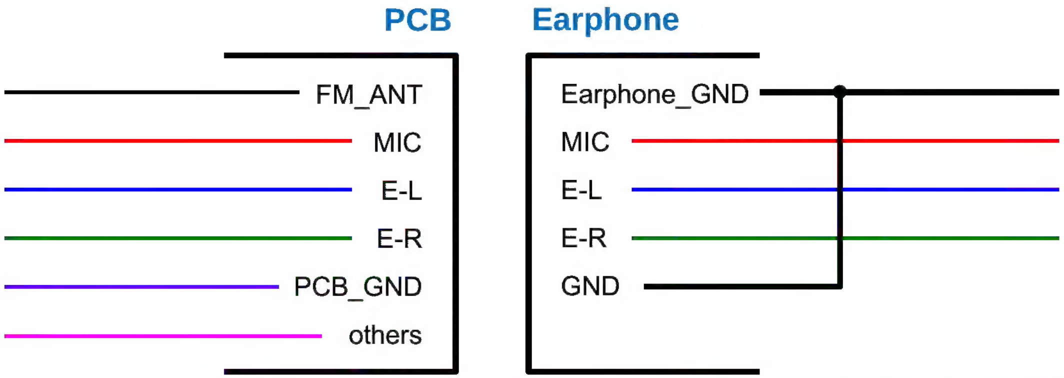
FM Earphone Antenna Pin Definition (2/3)

- Some **incorrect** pin definitions
  - Case 1: Floating FM_ANT pin



  - Case 2: Earphone_GND connects to both FM_ANT pin and PCB_GND



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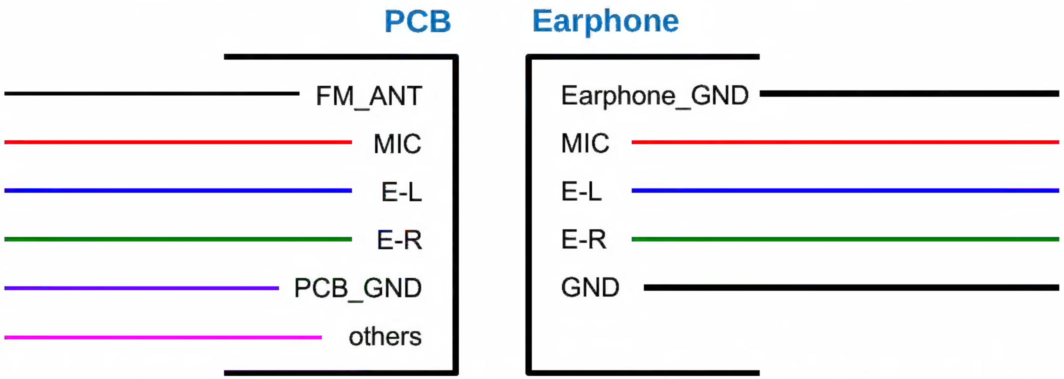
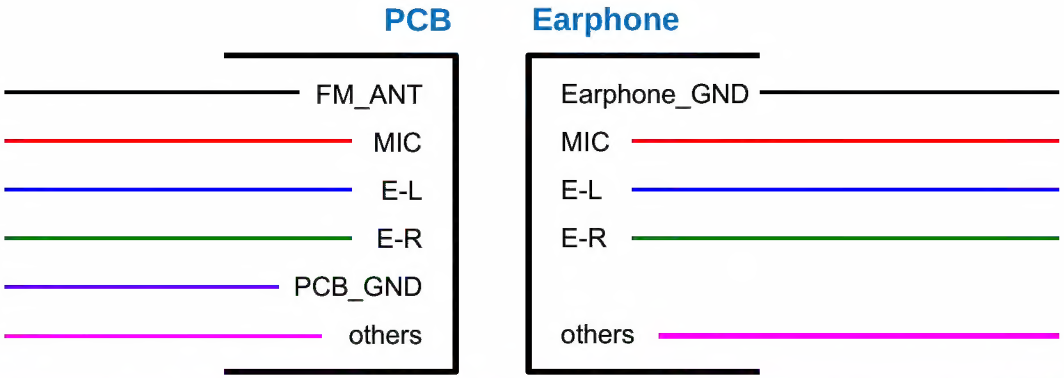
FM Earphone Antenna Pin Definition (3/3)

- Some incorrect pin definitions
  - Case 3: Unnecessary GND pin used on the earphone side



  - Case 4: Unnecessary signal pins used on the earphone side



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FM Earphone Antenna Troubleshooting

- Simple troubleshooting techniques:
  a. Check that only four earphone pins are used. (Case 3, Case 4)
  b. Remove the 22 uH inductor.
  c. Plug in the earphone.
  d. Use a digital multimeter to check whether the connections between **PCB_GND**, **FM_ANT** pin, and **Earphone_GND** pin are **OPEN** or **SHORT**.

FM_ANT to Earphone_GND	FM_ANT to PCB_GND	PCB_GND to Earphone_GND	Issue
SHORT	OPEN	OPEN	**Correct**
OPEN	OPEN	SHORT	**Case 1**
SHORT	SHORT	SHORT	**Case 2**

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